FACULTY VITAE

Name – Jegadeeshwari P

Education –

M.Tech, VLSI Design, Sathyabama University, Chennai, 2012.

B.E., Electronics & Communication Engineering, Thanthai Periyar Government Institute of Technology, Vellore,2001.

Academic experience –

Dr. M. G. R. Educational &Research Institute Assistant Professor, 2023-Present.

Worked as an Assistant Professor in CK College of Engineering and Technology, Cuddalore from December 2011 to March 2023.

Non-academic experience – NIL

Certifications or professional registrations- NIL

Current membership in professional organizations

Life time membership in Indian Society for Technical Education, New Delhi. Membership ID: LM114841.

Honors and awards- NIL

Service activities (within and outside of the institution) –

Faculty Development Coordinator

Women Development cell Convener

Academic Staff College Coordinator

Briefly list the most important publications and presentations from the past five years –

Jegadeeshwari P, et. al., (2023)," Fault Identification in Modified Hybrid Digital Pulse Width Modulation using Triple Modular Redundancy", WSEAS Transactions on Circuits and Systems DOI: 10.37394/23201.2023.22.16Emotion Tracker: Real-time Facial Emotion Detection with Open CV and Deep Face Year: 2023 | Conference Paper | Publisher: IEEE

Jegadeeshwari P, et. al., (2023)," FPGA implementation of KNN Algorithm-Based Prediction for DPWM Methods", Tuijin Jishu/Journal of Propulsion Technology-ISSN: 1001-4055-Vol. 44 No. 3.

Jegadeeshwari P, et. al., (2023)," Design of Integrated Digital PWM in Quantum Dot Cellular automata" -272-Chinese Journal of Computational Mechanics | 2023 | Issue 5

Jegadeeshwari P, et. al., (2022)," Digital Design of Counter based Pulse Width Modulation in Quantum dot Cellular Automata", IEEE International Conference on Smart Technologies and Systems for Next Generation Computing (ICSTSN).

Jegadeeshwari P, et. al., (2022)," Design of Fusion Digital Pulse Width Modulation in Quantum Dot Cellular Automata",10th International Conference on Contemporary Engineering and Technology (ICCET).

Jegadeeshwari P, et. al., (2021)," Performance Analysis of a novel Fusion Adder/ Subtractor design", Journal of Physics: Conference Series (Scopus).

Briefly list the most recent professional development activities-

Seminar on 'Outstanding in Teaching and Research' on July 3, 2024, Dr. M.G.R. Educational and Research Institute, Chennai.

Attended ten days Online FDP on "Designing chips with low power artificial intelligence " from 22.04.2024 to 01.05.2024 in collaboration with NIT, Warangal, and Dr.M.G.R. Educational and Research Institute.

DST-SERB Sponsored two days' workshop on "Artificial Intelligence and IoT Applications in Health Care from 27.12.2023 & 28.12.2023, Dr. M.G.R Educational & Research Institute.

Virtual FDP on “VLSI Design” from 18.12.2023 to 23.12.2023 Dr. M.G.R. Educational & Research Institute, Chennai.

Six Days Online FDP On High Performance VLSI Architectures for Multidisciplinary Applications Held From 31-07-2023 to 05-08-2023, SRM Institute of Science and Technology Faculty of Engineering and Technology, Chennai.

Online FDP On VLSI To System Design: Silicon to End Application Approach, 31.07.23 to 04.08.23 Organized By AICTE, New Delhi.