Dr. M.G.R.
EDUCATIONAL AND RESEARCH INSTITUTE
UNIVERSITY
(Decl. U/S 3 of the UGC Act 1956)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech. APPLIED ELECTRONICS (Part Time)
CURRICULUM and SYLLABUS
2013 Regulation

I SEMESTER						
S.No	**Subject code**	**Title of the Subject**	**L**	**T**	**P**	**C**
1	MMA130006	Applied Mathematics for Electronics Engineers	3	1	0	4
2	MEC13A001	Advanced Digital Signal Processing	3	0	0	3
3	MEC13A003	Advanced Digital System Design	3	0	0	3
		Total	**9**	**1**	**0**	**10**

II Semester						
S.No	**Subject code**	**Title of the Subject**	**L**	**T**	**P**	**C**
1	MEC13A004	Microcontroller Based System Design	3	0	0	3
2	MEC13A002	Analysis and Design of Analog ICs	3	0	0	3
3	MEC13V001	VLSI Architecture and Design Methodologies	3	1	0	4
4	MEC13AL01	Electronics Design Laboratory	0	0	3	2
		Total	**9**	**1**	**3**	**12**

III Semester						
S.No	**Subject code**	**Title of the Subject**	**L**	**T**	**P**	**C**
1	MEC13C001	High Performance Networks	3	0	0	3
2	MEC13V004	VLSI Signal Processing	3	0	0	3
3	MEC13V005	Embedded Systems	3	0	0	3
		Total	**9**	**0**	**0**	**9**

IV Semester						
S.No	**Subject code**	**Title of the Subject**	**L**	**T**	**P**	**C**
1	MEC13A005	Digital Image Processing	3	0	0	3
2	MEC13A006	Computer Architecture and Parallel Processing	3	0	0	3
3	MEC13AEXX	Elective – I	3	0	0	3
4	MEC13AL02	Term Paper	0	3	0	2
		Total	**9**	**3**	**0**	**11**

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V SEMESTER						
S.No	**Subject code**	**Subject**	**L**	**T**	**P**	**C**
1	MEC13A007	Digital Control Engineering	3	0	0	3
2	MEC13A008	Neural Networks and its Applications	3	0	0	3
3	MEC13AEXX	Elective – II	3	0	0	3
4	MEC13AL03	Project Phase – I	0	0	9	6
		Total	**9**	**0**	**9**	**15**

VI Semester						
S.No	**Subject code**	**Title of the Subject**	**L**	**T**	**P**	**C**
1	MEC13AEXX	Elective – I	3	0	0	3
2	MEC13VL04	Project Work & Viva Voce	0	0	24	15
		Total	**9**	**3**	**0**	**18**

Total Credits: 75

ELECTIVES						
S.No	**Subject code**	**Subject**	**L**	**T**	**P**	**C**
1	MEC13AE01	Modern Digital Communication Techniques.	3	0	0	3
2	MEC13V012	ASIC Design.	3	0	0	3
3	MEC13C009	Soft Computing.	3	0	0	3
4	MEC13AE04	Bio-Medical Instrumentation.	3	0	0	3
5	MEC13AE02	Microwave Integrated Circuits .	3	0	0	3
6	MEC13CE01	Multimedia Compression Techniques.	3	0	0	3
7	MEC13C003	Optical Communication Systems & Networks.	3	0	0	3
8	MEC13AE03	Synthesis and Optimization of Digital Circuits	3	0	0	3
9	MEC13CE07	Computer Communication and ISDN	3	0	0	3
10	MEC13C008	Electromagnetic Interference and Compatibility in System Design	3	0	0	3
11	MEC13CE05	High Speed Switching Architecture	3	0	0	3
12	MEC13VE03	Embedded Linux	3	0	0	3

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MMA130006 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS 3 1 0 4

OBJECTIVES

- To enable the students to learn the basic concepts of random process and special functions

UNIT – I ADVANCED MATRIX THEORY 12 Hrs

Generalized Eigen vectors-Jordan canonical form –Matrix Norms-QR algorithm-Pseudo Inverse-Singular value decomposition –Least Square Solutions.

UNIT – II RANDOM PROCESS 12 Hrs

Classification of Random Process-Stationary Process-Ergodic Process-Markov Process –Markov Chains-Auto Correlation –Auto Covariance –Cross Correlation-Cross Covariance-Spectral Density.

UNIT – III SPECIAL FUNCTIONS 12 Hrs

Bessel's Equation-Bessel Functions-Recurrence relations-Generating function-Orthogonal property-Legendre's equation-Legendre Polynomials- Rodrigue's formula.

UNIT – IV CALCULUS OF VARIATIONS 12 Hrs

Variation and its properties-Euler's equations- Functional dependent on First and Higher Order Derivatives- Functional depend on functions of several independent variables-Problems with moving boundaries-Direct methods-Ritz and Kantorovich methods.

UNIT – V INTEGRAL EQUATIONS 12 Hrs

Types of Integral equations-Fredholm Integral equation-Volteera Integral equation-Green's function- Fredholm Integral equations with Separable kernels- Iterative methods solving equations of second kind- Properties of Symmetric kernels.

Total No. of Hours: 60

References:

1. Bronson R., "*Theory and problems of Matrix Operations"* (Schaum's Outline Series),McGrawHill,(1989)
2. Lewis D.W., *"Matrix theory"*,Allied publishers,(1995)
3. Richard Johnson A., *"Miller & Freund's Probability and Statistics for Enginners"*(8th ed.) Prentice Hall of India(2009)
4. Veerarajan T., *"Probability Statistics and Random Process"* , Tata McGraw Hill Publishing Co.,(2008)
5. Venkataraman M.K., " *Higher Mathematics for Engineering and Science"* , The National Publishing Co.,(2006)
6. Gupta A.S., *"Calculus of variations with applications"*, Prentice Hall of India,(2004)
7. Raisinghania M.D., *"Integral Equations and Boundary Value Problems"* (3^{rd} ed),S.Chand & Co., (2010)
8. Hildebrand F.B., *"Methods of Applied Mathematics*" , Dover Books,(1992)

MEC13A003 ADVANCED DIGITAL SYSTEM DESIGN 3 0 0 3

OBJECTIVES

- To enable the students the ability to design complex sequential circuits
- To equip the students with the ability to detect and correct faults using various algorithms

UNIT -I SEQUENTIAL CIRCUIT DESIGN 9 Hrs

Analysis of Clocked Synchronous Sequential Networks (CSSN), Modeling of CSSN, State Stable Assignment and Reduction, Design of CSSN, Design of Iterative Circuits, ASM Chart, ASM Realization, Design of Arithmetic circuits for Fast adder- Array Multiplier.

UNIT- II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9 Hrs

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits.

UNIT-III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9 Hrs

Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test.

UNIT- IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9 Hrs

Programming Techniques -Re-Programmable Devices Architecture- Function blocks, I/O blocks, Interconnects, Realize combinational, Arithmetic, Sequential Circuit with Programmable Array Logic; Architecture and application of Field Programmable Logic Sequence.

UNIT -V NEW GENERATION PROGRAMMABLE LOGIC DEVICES 9 Hrs

Fold back Architecture with GAL, EPLD, EPLA, PEEL, PML; PROM – Realization State Machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 - Xilinx 3000

Total No. of Periods: 45

References:

1. Donald G. Givone, "*Digital principles and Design*", Tata McGraw Hill 2002.
2. Stephen Brown and Zvonk Vranesic, "*Fundamentals of Digital Logic with VHDL Deisgn*", Tata McGraw Hill, 2002
3. Mark Zwolinski, "*Digital System Design with VHDL*", Pearson Education, 2004
4. Parag K Lala, "*Digital System design using PLD*", BS Publications, 2003
5. John M Yarbrough, *"Digital Logic applications and Design*", Thomson Learning, 2001.
6. Nripendra N Biswas, "*Logic Design Theory*", Prentice Hall of India, 2001

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MEC13A001 ADVANCED DIGITAL SIGNAL PROCESSING 3 0 0 3

OBJECTIVES

- To enable the students to get the fundamentals of parametric and non-parametric analysis
- To enable the students to design adaptive filters using different methodologies

UNIT –I DISCRETE RANDOM SIGNAL PROCESSING 9 Hrs

Discrete Random Process, Expectation, Variance, Co-Variance, Scalar Product, Energy of Discrete Signal-Parseval's Theorem, Wiener Khintchine Relation-Power Spectral Density –Periodogram – Sample Autocorrelation-Sum Decomposition Theorem, Spectral Factorization Theorem – Discrete Random Signal Processing by Linear Systems-Simulation of White Noise – Low Pass Filtering of White Noise.

UNIT – II SPECTRUM ESTIMATION 9 Hrs

Non-Parametric Methods-Correlation Method – Co-Variance Estimator – Performance Analysis of Estimators – Unbiased, Consistent Estimators – Periodogram Estimator – Bartlett Spectrum Estimation – Welch Estimation – Model based Approach – AR, MA, and ARMA Signal Modeling – Parameter Estimation using Yule-Walker Method.

UNIT – III LINEAR ESTIMATION AND PREDICTION 9 Hrs

Maximum likelihood criterion-efficiency f estimator – Least mean squared error criterion – Wiener filter – Discrete Wiener Hoff equations – Recursive estimators-Kalman filter – Linear prediction, prediction error-whitening filter, inverse filter – Levinson recursion, Lattice realization, and Levinson recursion algorithm for solving Teoplitz system of equations.

UNIT – IV ADAPTIVE FILTERS 9 Hrs

FIR adaptive filters – Newton's steepest descent method-adaptive filter based on steepest descent method – Widrow Hoff LMS adaptive algorithm – Adaptive channel equalizations – Adaptive echo chancellor – Adaptive noise cancellation – RLS adaptive filters –Exponentially weighted RLS – sliding window RLS – Simplified IIR LMs adaptive filter

UNIT – V MULTI RATE DIGITAL SIGNAL PROCESSING 9 Hrs

Mathematical description of change of sampling rate – Interpolation and Decimation –continuous time model – Direct digital domain approach -Decimation by an integer factor – Interpolation by an integer factor – single and multistage realization - Poly phase realization – Application to sub band coding – Wavelet transform and filter bank implementation of wavelet expansion of signals.

Total No. of Hours: 45

References:

1. Monson H. Hayes, "*Statistical Digital Signal Processing and Modeling*", John Wiley and Sons, Inc., New York, 1996
2. John G. Proakis, Dimitris G. Manolais, "*Digital Signal Processing Prentice Hall of India*", 1995.
3. Sopocles J. Orfanidis, "*Optimum Signal Processing*", McGraw Hill, 1990.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MEC13A002 ANALYSIS AND DESIGN OF ANALOG IC'S 3 0 0 3

OBJECTIVES

- To enable the students to design and analyze various analog circuits using op-amps and IC's

UNIT –I CIRCUIT CONFIGURATION FOR LINEAR IC 13 Hrs

Current Sources, Analysis of Difference Amplifiers with Active load, Supply and Temperature Independent Biasing Technique Voltage References.

UNIT – II OPERATIONAL AMPLIFIERS 10 Hrs

Analysis of Operational Amplifier Circuits, Slew Rate Model and High Frequency Analysis, Operational Amplifier Noise Analysis.

UNIT – III ANALOG MULTIPLIER AND PLL 10 Hrs

Analysis of four Quadrant and Variable Trans-conductance Multiplier, Voltage Controlled Oscillator, Closed loop Analysis of PLL.

UNIT –IV MOS ANALOG ICS 6 Hrs

Design of MOS Operational Amplifier, MOS Power Amplifier.

UNIT – V MOS SWITCHED CAPACITOR FILTERS 6 Hrs

Design Techniques for Switched Capacitor Filter.

Total No. Of Periods: 45

References:

1. Behazad Razavi, "*Principles of Data Conversion System Design*", S.Chand & Company Ltd, 2000.
2. Grey and Meyer, "*Analysis and Design of Analog Ics*." Wiley International, 1996.
3. Kenneth R.Laker, Willy M.C.Sansen, William M.C.Sansen, "*Design of Analog Integrated Circuits and Systems*", McGraw Hill, 1994
4. Grey, Wolley, Brodersen, "*Analog MOS Integrated Circuits*", IEEE Press, 1989.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MEC13V001 VLSI ARCHITECTURE AND DESIGN METHODOLOGIES 3 1 0 4

OBJECTIVES

- To enable the students to absorb the concepts of different PLDs
- To enable the students to equip with the different ASIC and FPGA Techniques

UNIT- I CMOS DESIGN 12 Hrs

Overview of Digital VLSI Design Methodologies- Logic Design with CMOS-Transmission gate Circuits-Clocked CMOS-Dynamic CMOS Circuits, Bi-CMOS Circuits- Layout Diagram,Stick Diagram-IC Fabrications – Trends in IC Technology.

UNIT- II PROGRAMABLE LOGIC DEVICES 12 Hrs

Programming Techniques-Anti fuse-SRAM-EPROM and EEPROM Technology –Re-Programmable Devices Architecture- Function Blocks, I/O Blocks, Interconnects, Xilinx- XC9500,Cool Runner - XC-4000,XC5200, SPARTAN, Virtex - Altera MAX 7000- Flex 10K-Stratix.

UNIT- IIIASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 12 Hrs

System Partition – FPGA Partitioning – Partitioning Methods- Floor Planning – Placement Physical Design Flow – Global Routing – Detailed Routing – Special Routing- Circuit Extraction – DRC.

UNIT- IV ANALOG VLSI DESIGN 12 Hrs

Introduction to Analog VLSI- Design of CMOS 2stage-3 Stage Op-Amp –High Speed and High Frequency Op-Amps-Super MOS-Analog Primitive Cells-Realization of Neural Networks.

UNIT -V LOGIC SYNTHESIS AND SIMULATION 12 Hrs

Overview of Digital Design with Verilog HDL, Hierarchical Modeling Concepts, Modules and Port Definitions, gate Level Modeling, Data Flow Modeling, Behavioral Modeling, Task & Functions, Verilog and Logic Synthesis-Simulation-Design examples, Ripple carry Adders, Carry Look ahead Adders, Multiplier, ALU, Shift Registers, Multiplexer, Comparator, and Test Bench.

Total No. Of Periods: 60

References Books:

1. M.J.S Smith, "*Application Specific integrated circuits*",Addition Wesley Longman Inc.1997.
2. Kamran Eshraghian,Douglas A.pucknell and Sholeh Eshraghian*,"Essentials of VLSI circuits and system*", Prentice Hall India,2005.
3. Wayne Wolf, *"Modern VLSI design*" Prentice Hall India, 2006.
4. Mohamed Ismail, Terri Fiez, *"Analog VLSI Signal and information Processing*", McGraw Hill International Editions,1994.
5. Samir Palnitkar, "*VeriLog HDL, A Design guide to Digital and Synthesis*" 2nd Ed, Pearson, 2005.

MEC13A004 MICROCONTROLLER BASED SYSTEM DESIGN 3 0 0 3

OBJECTIVES

- To enable the students to design microcontroller based embedded systems
- To enable the students to develop real-time peripheral applications

UNIT – I 8051 MICROCONTROLLER 9 Hrs

Intel 8051 Architecture – Hardware – I/O ports – External Memory – Counters and Timer – Serial data I/O – Interrupts, Assembly language, Addressing Modes, Instruction Set - Simple Programs, 8051 Interfacing to LCD, ADC, DAC and Stepper Motors.

UNIT- II 68HC11 MICROCONTROLLER 9 Hrs

Motorola 68HC11 Architecture – Input / Output Ports – Resets and Self Protection – Interrupt Timing – A/D, D/Converters.

UNIT – III 8096 MICROCONTROLLER 9 Hrs

Intel 8096 CPU Structure, I/O Ports – Register File – Assembly Language – Addressing modes – Instruction set – Simple Programs.

UNIT – IV REAL TIME CONTROL PROGRAMMING 9 Hrs

Interrupt Structure – Programmable Timers – Real Time Clock Latency – Interrupt Density and Interval Consideration, Shared Resources and Critical Regions.

UNIT – V SOFTWARE AND EXPANSION METHODS 9 Hrs

Queues – Table and Strings – Program Organization – State Machines – Key Switch Parsing – Timing Consideration – UART Ports – I/P O/P Serial Ports Programmable Controllers.

Total Number of Hours: 45

References:

1. Kenneth J.Ayala, "*The 8051 Microcontroller Architecture, Programming & Applications*" – Penram International publishing (India), Second Edition, 1996.
2. Muhammed Ali Mazidi, Janice Gillies Pie Mazidi, "*The 8051 Microcontroller and Embedded Systems*"– Pearson EducationAsia.
3. PEATMAN J.B, "*Design with Microcontrollers*" – McGraw Hill Book International Ltd, Singapore, 1989.
4. Intel Manual on 16 – bit *"Embedded controllers*", Santa Clara, 1991.

MEC13AL01	ELECTRONICS DESIGN LABORATORY	0	0	3	2

OBJECTIVES

- To enable the students to design digital systems using 16 bit microprocessors and analog systems using EDA tools

1. SCHEMATIC CAPTURE AND PCB LAYOUT DESIGN USING EDA TOOLS.
2. SYSTEM DESIGN USING MICRO CONTROLLERS.
3. MICROCONTROLLER BASED TIMERS, STEPPER MOTOR CONTROLLER, LCD & CRT INTERFACING
4. SYSTEM DESIGN USING 16 BIT MICROPROCESSORS.
5. SPICE SIMULATION OF ELECTRONIC CIRCUITS.
6. DESIGN OF POWER ELECTRONIC CIRCUITS – SMPS, HIGH FREQUENCY DC/DC CONVERTERS USING POWER MOSFET

MEC13C001 HIGH PERFORMANCE NETWORKS 3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts of TCP/IP, ATM and Wireless Networks and its applications in real time system design.

UNIT – I BASICS OF NETWORKS 9 Hrs

Telephone, Computer, Cable Television and Wireless Network, Networking principles, Service integration, Network services and Layered Architecture, Traffic Characterization and QOS. Networks services: Network Elements and Network Mechanisms.

UNIT – II PACKET SWITCHED NETWORKS 9 Hrs

OSI and IP Models: Ethernet (IEEE 802.3): Token Ring (I EEE 802.5), FDDI, DQDB, frame relay: SMDS: Internetworking with SMDS, 802.11 Standards & their deployment

UNIT – III INTERNET AND TCP/IP NETOWRKS 9 Hrs

Overview, Internet Protocol: TCP/IP: Performance of TCP/IP Networks-Circuit Switched Networks: SONET; DWDM, Fiber To home, DSL. Intelligent Networks, CATV.

UNIT – IV ATM AND WIRELESS NETWORKS 9 Hrs

Main features – Addressing, Signaling and Routing: ATM Head Restructure – Adaption Layer, Management and Control: BISDN; Internetworking with ATM.

UNIT –V OPTICAL NETWORKS AND SWITCHING 9 Hrs

Optical links – WDM systems, Cross – Connects, Optical LAN's optical paths and networks: TDS and SDS: Modular switch design Packet switching, Distributed, Shared, Input, and output Buffers.

Total No. Of Periods: 45

References:

1. Jean Warland and Pravin Varaiya, "*High, Performance Communication Networks*", 2nd Edition, Harcourt and Morgan Kauffman, London, 2000.
2. Leon Gracia, Widjaja, "*Communication Networks*", Tata McGraw Hill, New Delhi, 2000.
3. Behrouz.a. Forouzan, "*Data Communication and Networking*", Tata McGraw Hill, New Delhi, 2000.

MEC13V004 VLSI SIGNAL PROCESSING 3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts of parallel processing, pipelining and various fast convolution techniques

UNIT – I PIPELINING AND PARALLEL PROCESSING: 8 Hrs

Introduction - Pipelining of FIR Digital filters - Parallel Processing - Pipelining and Parallel Processing for Low Power.

UNIT – II RETIMING AND UNFOLDING 12 Hrs

Introduction - Definitions and Properties - Solving System of Inequalities - Retiming Techniques. Introduction - An Algorithm for Unfolding - Properties of Unfolding - Critical Path, Unfolding and Retiming - Application of Unfolding.

UNIT – III SYSTOLIC ARCHITECTURE DESIGN: 9 Hrs

Introduction - Systolic Array Design Methodology - FIR Systolic Arrays - Selection of Scheduling Vector - Matrix Multiplication and 2D Systolic Array Design - Systolic Design for Space Representations Containing Delays .

UNIT – IV FAST CONVOLUTION: 8 Hrs

Introduction - Cook - Toom Algorithm - Winograd Algorithm - Iterated Convolution - Cyclic Convolution - Design of Fast Convolution Algorithm by Inspection.

UNIT – V SCALING AND ROUNDOFF NOISE 8 Hrs

Introduction – Scaling and Round off Noise – State Variable Description of Digital Filters – Scaling and Round off Noise Computation – Round off Noise in Piplined IIR filter – Round off Noise Computation Using State variable description – Slow down, retiming, and pipelining

Total No. of Periods: 45

References:

1. Keshab. K. Parhi, "*VLSI Digital signal processing systems -Design and Implementations*" Wiley - Inter science, 1999.
2. Mohammed Ismail, Terri, Fiez, "*Analog VLSI signal and Information Processing*", 1994 McGraw Hill.
3. Kung .S.Y, H.J. While house, T. Kailath, *"VLSI and Modern signal processing*", Prentice hall, 1985
4. Jose E. France, Yannis Tsividis "*Design of Analog - Digital VLSI circuits for Telecommunications and signal processing"* - Prentice Hall, 1994.

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MEC13V005 EMBEDDED SYSTEMS 3 0 0 3

OBJECTIVES

- To enable the students to learn the design issues in microcontrollers and their performance metrics.

UNIT – I 68HC11 AND 8051 MICROCONTROLLER 9 Hrs

Embedded Computer systems: - Applications, Software issues, Memory Mapped Architecture, 68HC11 Architecture and Different Addressing Modes, Study of Intel 8051 Microcontroller Architecture and Instruction Set

UNIT – II PIC MICROCONTROLLER 9 Hrs

Programming of PIC Micro Controllers. Architecture of PIC Micro Controllers. Instruction Set of PIC Micro Controllers. Simple Assembly language and C Program for PIC Microcontroller

UNIT – III SOFTWARE DEVELOPMENT 9 Hrs

Software Development: - Quality Programming, Memory Allocation, Self-Documenting Code, Abstraction, Modular Software Development Device Drivers, Threads Recursion

UNIT – IV 9 Hrs

Interfacing method.

Blind Cycle Counting Synchronization, Gadfly Synchronization, Printer Interfacing

Interrupt Synchronization:

Reentrant programming, FIFO Queue, 6811 Interrupts Polled Versus Vectored Interrupts

Timing Generation and Measurements

MC8811 Input Capture, Period Measurements, Output Compare, Square Wave Generation Frequency Measurements.

UNIT – V 9 Hrs

Serial I/O devices: RS232 Specifications, Communication Protocols, MC6811 SCI ad SPI. **Parallel port Interfaces:** Input Switches and Keyboard, output LED, Stepper Motor. **Memory Interfacing:** Address Switching, Memory Interface, examples for MC6H16, Introduction to High speed I/O Interfacing.

References: **Total No. of Periods: 45**

1. Jonathan.W.Valvano, *"Embedded Microcomputer system"*, Brooks/COLE Thomson learning series
2. John B Peatman "*Design with PIC Microcontroller*" Latest Edison.
3. Myke Predko TMH. "*Programming and customizing the Microcontroller*"

MEC13A005 DIGITAL IMAGE PROCESSING 3 0 0 3

OBJECTIVES

- To enable the students to learn the various digital image processing techniques

UNIT – I CONTINOUS AND DISCRETE IMAGES AND SYSTEMS 9 Hrs

Light, Luminance, Brightness and Contrast, Eye, The Monochrome Vision Model, Processing Problems and Applications, Vision Camera, Digital Processing System, 2-D sampling Theory, Aliasing, Image Quantization, Lloyd Max Quantizer, Dither, Color Images, Linear Systems And Shift Invariance, Fourier Transform, Z-Transform, Matrix theory Results, Block Matrices and Kronecker Products.

UNIT – II IMAGE TRANSFORMS 9 Hrs

2-D orthogonal and Unitary transforms, 1-D and 2-d DFT, Cosine, Sine, Walsh, Hadamard, Haar, Slant, Karhunen-loeve, singular value Decomposition transforms.

UNIT – III IMAGE ENHANCEMENT 9 Hrs

Point operations – Contrast Stretching, Clipping and thresholding Density Slicing, Histogram Equalization, Modification and Specification, Spatial Operations – Spatial Averaging, low pass, high pass, band pass filtering, Direction Smoothing, Medium Filtering, Generalized Cepstrum and Homomorphic Filtering, Edge enhancement using 2-D IIR and FIR filters, color Image Enhancement

UNIT –IV IMAGE RESTORATION 9 Hrs

Image Observation Models, Sources of Degradation, Inverse and Wiener Filtering, Geometric mean Filter, Non-linear Filters. Smoothing Splines and Interpolation, Constrained least Squares Restoration.

UNIT – V IMAGEDATA COMPRESSION AND IMAGE RECONSTRUCTION FROM PROJECTION 9 Hrs

Image Data Rates, Pixels Coding, Predictive Techniques Transform Coding and Vector DPCM, Block Truncation Coding, wavelet Transform Coding of images, Color image Coding. Radon Transform.

Total Number of Periods: 45

References:

1. Anil K. Jain, "*Fundamentals of Digital Image Processing*", PHI 1995.
2. M.A. Sid Ahmed, "*Image Processing*", McGraw Hill, Inc, 1995.
3. R.Gonzalazand P.Wintz, "*Digital Image Processing*", Addition Wesley 2nd Ed, 1987.
4. William. K.Pratt, "*Digital Image Processing*", Wiley Interscience, 2nd Ed, 1991.

MEC13A006 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts of parallel processing and their performances

UNIT – I THEORY OF PARALLELISM **9 Hrs**

Parallel Computer models – the state of Computing, Multiprocessors and Multicomputer and Multivectors and SIMD Computers, PRAM and VLSI models, Architectural Development Tracks, Program and Network Properties – Conditions of Parallelism.

UNIT – II PARTITIONING AND SCHEDULING **9 Hrs**

Program Partitioning and Scheduling, Program Flow Mechanisms, System Interconnect Architectures, Principles of Scalable Performance – Performance Matrices and Measures, Parallel Processing Applications, Speedup Performance laws, Scalability Analysis and Approaches.

UNIT – III HARDWARE TECHNOLGIES **9 Hrs**

Processor and Memory Hierarchy Advanced Processor Technology, Superscalar and Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology, Bus Cache and Shared Memory – Backplane bus systems, Cache Memory Organizations, Shared memory Organizations, Sequential and Weak Consistency Models.

UNIT – IV PIPELINING AND SUPERSCALAR TECHNOLOGIES **9 Hrs**

Parallel and Scalable architectures, Multiprocessor and Multicomputer, Multifactor and SIMD Computers, Scalable, Multithreaded and data flow architectures.

UNIT – V SOFTWARE AND PARALLEL PROCESSING **9 Hrs**

Parallel Models, Languages and Compilers, Parallel Program Development and Environments, UNIX, MACH and OSF/1 for Parallel Computers.

Total Number of Periods : 45

References:

1. Kai Hwang "*Advanced Computer Architecture*". McGraw Hill International 2001.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, "*Advanced computer Architecture – A design Space Approach*". Pearson Education,2003.
3. Carl Homacher, Zvonko Vranesic, Sefwat Zaky, "*Computer Organisation", 5th Edition, TMH, 2002.*
4. David E. Culler, Jaswinder Pal Singh with Anoop Gupta "*Parallel Computer Architecture*", Elsevier, 2004.
5. John P. Shen. "*Modern processor design Fundamentals of super scalar processors*", Tata McGraw Hill 2003.
6. Sajjan G. Shiva "*Advanced Computer Architecture*", Taylor & Francis, 2008.

MEC13A007 DIGITAL CONTROL ENGINEERING 3 0 0 3

OBJECTIVES

- To equip the students with the design of digital PID Controllers

UNIT – I PRINCIPLES OF CONTROLLERS 9 Hrs

Review of Frequency and Time Response Analysis and Specifications of Control Systems, Need For Controllers, Continues Time Compensations, Continues Time PI, PD, PID controllers, digital PID controllers.

UNIT – II SIGNAL PROCESSING IN DIGITAL CONTROL 9 Hrs

Sampling, Time and Frequency Domain Description, Aliasing, Hold operation, Mathematical model of sample and hold, Zero and first order hold, Factors limiting the choice of sampling rate, Reconstruction.

UNIT – III MODELLING AND ANALYSIS OF SAMPLED DATA CONTROL LANGUAGE 9 Hrs

Difference equation description, Z-transform method of description, Pulse transfer function, Time and frequency response of discrete time control systems, Stability of digital control systems, Jury's stability test, State variable concepts, First companion, Second companion, Jordan canonical models, Discrete state variable models, Elementary principles.

UNIT – IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9 Hrs

Review of principle of compensator design Z-plane specification, Digital Compensator design using frequency response plots, discrete integrator, Discrete Differentiator, Development of Digital PID controller, Transfer function, Design in The Z – Plane.

UNIT –V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9 Hrs

Algorithm development of PID control algorithms, Software implementation, Implementation using Microprocessors and Microcontrollers, Finite word length effects, Choice of data acquisition systems, Microcontroller based temperature control systems, Microcontroller based motor speed control systems.

References:

Total No. Of Periods: 45

1. M.Gopal, "*Digital control and static variable Methods*", Tata McGraw Hill, New Delhi, 1997.

2. John J. D' Azzo, "*Constantine Houpios, Linear Control System Analysis nad Design*", McGraw Hill, 1995.
3. Kenneth J. Ayala, "*The 8051 Microcontroller – Architecture, Programming and Application*", Penram International, 2nd Edition, 1996.

MEC13A008 NEURAL NETWORKS AND ITS APPLICATIONS 3 0 0 3

OBJECTIVES

- To equip the students with the design of neural networks using various algorithms and their applications

UNIT – I INTRODUCTION TO ARTIFICIAL NEURAL NETWORKS 9 Hrs

Neuro – Physiology – General Processing Element – Adaline – LMS learning rule – MADALINE – perception Networks

UNIT – II BPN AND BAM 9 Hrs

Back Propagation Network – Updating of output and hidden layer weights – Application of BPN – Associative memory – Bi-directional Associative Memory - Hop field memory – Traveling sales man problem

UNIT – III SIMULATED ANNEALING AND CPN 9 Hrs

Annealing, Boltzmann machine – Learning – Application – Counter Propagation network – Architecture – Training – Application.

UNIT –IV SOM, ART & NEOCOGNITRON 9 Hrs

Self-organizing map – Learning algorithm – Feature map classifier – Applications – Architecture of Adaptive Resonance theory – Pattern matching in ART network. Neocognitron: Architecture of Neocognitron – Data processing and performance of architecture of Spacio – Temporal networks for speech recognition

UNIT – V CASE STUDY: 9 Hrs

1. Implementation of BPN algorithm in a computer language
2. Application of Neural Networks for Pattern recognition, data comparison
3. Hop field networks for n-bit A/D converter

Total No. of Periods: 45

References:

1. J.A. Freeman and B.M. Skapura, "*Neural Networks, Algorithms Applications and Programming Techniques*", Addison-Wesley, 1990.
2. Laurence Fausett, "*Fundamentals of Neural Networks: Architecture, Algorithms and Applications*", Prentice Hall, 1994.

MEC13AE01 MODERN DIGITAL COMMUNICATION TECHNIQUES 3 0 0 3

OBJECTIVES

- To equip the students with the techniques of coherent and non-coherent communication design

UNIT – I INTRODUCTION TO DIGITAL COMMUNICATION: 9 Hrs

Electromagnetic spectrum, ranges and application area. , channel types, characteristics and modeling. , analog and digital communications Functional architecture coded and encoded digital communication System architecture.

UNIT – II DIGITAL MODULATION 9 Hrs

Probability or error, phase modulated signals, baseband receiver and transmitter modules, Nyquist-pulse psk, Raised cosine Nyquist pulses, Quadrature modulation schemes PSD, Data pulse stream, M-ary Markov source, convolutionally coded modulation continuous phase.

UNIT – III COHERENT AND NON-COHERENT COMMUNICATION WAVEFORM 9 Hrs

Optimum coherent and non coherent receivers for cpfsk , Optimum ML coherent receiver for CPFSK , Optimum ML NON-coherent receiver for CPFSK , Analysis of simple non coherent receivers: Differential detection , Discriminator detection , Numerical results .Optical receiver in WGN, MF receiver, Matrix generation, colored GN, Whitening approach, in phase and Quadrature phase modern.

UNIT – IV BAND LIMITED CHANNELS 9 Hrs

Digital transmission through band limited channel, signal design for band limited channel,
the design of band limited signals for zero ISI, Optimum pulse shape design, Optimum demodulations of digital signals in the presence of ISI

UNIT – V CODED DIGITAL COMMUNICATION 9 Hrs

Architecture, interfacing, detailing, Synchronization, block coded digital communication system, performance, type of binary block codes, Shannon channel coding theorem, linear block codes.

Total No of periods: 45

References:

1. Simon Haykin, "*Digital Communications*", John Wiley and sons, 1998.
2. Wayne Tomasi, "*Advanced Electronic Communication System*", 4th Edition, Pearson Education Asia, 1998
3. B.P. Lathi, "*Modern Digital and Analog Communication Systems*", 3rd Edition, Oxford University Press, 1998.
4. M.K. Simon, S.M. Hindedi and W.C. Lindsey, "*Digital Communication Techniques: Signaling and Detection*", Prentice Hall India, New Delhi. 1995.

MEC13V012 ASIC DESIGN 3 0 0 3

OBJECTIVES

- To enable the students to understand and analyse the various types of ASICs and their design flow

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 12 Hrs

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND I\O CELLS 12 Hrs

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE ANDLOWLEVELDESIGNENTRY 12 Hrs

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 12 Hrs

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation, Introduction to JTAG.

UNIT-V ASIC CONSTRUCTION, FLOORPLANNING, PLACEMENT AND ROUTING 12Hrs

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

Total No. Of Hrs: 60

References:

1. M.J.S .Smith, "*Application - Specific Integrated Circuits* ", Addison -Wesley Longman Inc., 1997.
2. Andrew Brown, *" VLSI Circuits and Systems in Silicon*", McGraw Hill, 1991
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, "*Field Programmable Gate Arrays*" Kluwer Academic Publishers, 1992.

MEC13C009 SOFT COMPUTING 3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts of fuzzy algorithms and its applications in neural networks and artificial intelligent systems.

UNIT-I FUZZY SET THEORY 9 Hrs

Introduction to Neuro – Fuzzy and Soft Computing – Fuzzy Sets – Basic Definition and erminology – Set-theoretic Operations – Member Function Formulation and Parameterization – Fuzzy Rules and Fuzzy Reasoning – Extension Principle and Fuzzy Relations – Fuzzy If-Then Rules – Fuzzy Reasoning – Fuzzy Inference Systems – Mamdani Fuzzy Models – Sugeno Fuzzy Models – Tsukamoto Fuzzy Models – Input Space Partitioning and Fuzzy Modeling.

UNIT-II OPTIMIZATION 9 Hrs

Derivative-based Optimization – Descent Methods – The Method of Steepest Descent – Classical Newton's Method – Step Size Determination – Derivative-free Optimization –
Genetic Algorithms – Simulated Annealing – Random Search – Downhill Simplex Search.

UNIT- III NEURAL NETWORKS 9 Hrs

Supervised Learning Neural Networks – Perceptrons - Adaline – Back propagation Multi layer Perceptrons – Radial Basis Function Networks – Unsupervised Learning Neural Networks – Competitive Learning Networks – Kohonen Self-Organizing Networks – Learning Vector Quantization – Hebbian Learning.

UNIT -IV NEURO FUZZY MODELING 9 Hrs

Adaptive Neuro-Fuzzy Inference Systems – Architecture – Hybrid Learning Algorithm – Learning Methods that Cross-fertilize ANFIS and RBFN – Coactive Neuro Fuzzy Modeling – Framework Neuron Functions for Adaptive Networks – Neuro Fuzzy Spectrum.

UNIT -V APPLICATIONS OF COMPUTATIONAL INTELLIGENCE 9 Hrs

Printed Character Recognition – Inverse Kinematics Problems – Automobile Fuel Efficiency Prediction – Soft Computing for Color Recipe Prediction.

Total No. of periods: 45

References:

1. J.S.R.Jang, C.T.Sun and E.Mizutani, "*Neuro-Fuzzy and Soft Computing*", PHI, 2004, Pearson Education 2004.
2. Timothy J.Ross, "*Fuzzy Logic with Engineering Applications*", McGraw-Hill, 1997.
3. Davis E.Goldberg, "*Genetic Algorithms: Search, Optimization and Machine Learning*", Addison Wesley, N.Y., 1989.
4. S. Rajasekaran and G.A.V.Pai, "*Neural Networks, Fuzzy Logic and Genetic Algorithms*", PHI, 2003.

MEC13CE07 COMPUTER COMMUNICATION AND ISDN 3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts and design issues in communication networks.

UNIT – I COMPUTER COMMUNICATION 9 Hrs

Evolution of data Networks, Network architecture, ISO Reference model example of networks, Application of networks.

UNIT – II MEDIUM ACCESS SYBLAYER & DATA LINK LAYER 9 Hrs

Local area networks, conventional channel allocation methods, pure – ALOHA, S-ALOHA, finite population ALOHA , Controlled ALOHA, Reservation ALOHA, Design issues for packet radio networks- IEEE standards for LAN – Ethernet.

UNIT – III NETWORK AND TRANSPORT LAYER 9 Hrs

Network layer design issues – Routing algorithms- Congestion control algorithms – Internet working. Transport layer design issues – connection management

UNIT – IV QUEING THEORY AND CAPACITY ASSIGNMENT 9 Hrs

M/M/I Queues, M/G/I – Priority queuing capacity assignment for terminal network and distributed networks – concentration and buffering for finite and infinite buffers

UNIT – V PRESENTATION LAYER & APPLICATION LAYER 9 Hrs

Design issues – Abstract syntax notation – Data compression techniques – Cryptography – Remote procedure call. Design issues – file transfer access and managements.

Total No. of Periods: 45

References:

1. Andrew S. Tanenbaum,"*Computer Networks*" – Prentice Hall of India 1990.
2. D. Bertsekas and R. Gallagherv, "*Data Networks*" – Prentice hall of India, 1989.
3. Fred Halsall, "*Data Communication, Computer Networks and Open System*", Addition Welsey 2000.
4. Gerd E. Keiser, "*Load Area Networks*", McGraw Hill Publication, 1989.

MEC13AE04 BIOMEDICAL INSTRUMENTATION 3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts of biomedical instruments and their applications**.**

UNIT – I FUNDAMENTALS OF MEDICAL INSTRUMENTATION 9 Hrs

Anatomy and physiology-Physiological system of the body-Sources of biomedical signals-
Basic medical instrumentation system-Performance requirements of medical instrumentation system-Intelligent medical instrumentation system

UNIT – II BIOMEDICAL RECORDERS 9 Hrs

ECG-VCG-PCG-EEG-EMG-Other biomedical recorders-Biofeedback instrumentation

UNIT – III PHYSIOTHERAPY AND ELECTROTHERAPY EQUIPMENT 9 Hrs

High frequency heat therapy-Short wave diathermy-Microwave Diathermy-Ultrasonic therapy unit-
Pain relief through electrical stimulation-Diaphragm pacing by radiofrequency.

UNIT – IV VENTILATORS 9 Hrs

Mechanics of respiration-Artificial ventilation-Ventilators and its types –Ventilator terms –Classification of ventilators-Humidifiers-Nebulizers-Aspirators.

UNIT – V PATIENT SAFETY 9 Hrs

Electric shock hazards-Leakage currents-Safety codes for Electro medical equipment-Electrical safety analyzer-Testing of biomedical Equipment.

Total No. of Hours: 45

References:

1 KHANDPUR, "*Handbook on Bio-medical Instrumentation*"-Tata McGraw Hill Co Ltd., 1989
2 LESIS CROMWELL FRED, J.WERBELL and ERICH A.PFRAFFER, "*Bio-medical Instrumentation and measurements*"- Prentice Hall of India, 1990.

MEC13AE02 MICROWAVE INTEGRATED CIRCUITS 3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts of microwave IC's and their applications

UNIT – I MICROSTRIPS LINES, DESIGN, ANALYSIS 9 Hrs

Introduction, Types of MICs and their technology, Propagation models, Analysis of MIC y conformal transformation, Numerical analysis, Hybrid mode analysis. Losses in Micro strip, Introduction to slot line and coplanar wave guide

UNIT – II COUPLED MICROSTRIP, DIRECTIONAL COUPLERS AND LUMPED ELEMENTS FOR MICS 9 Hrs

Introduction to coupled Micro strip, Even and odd mode analysis , Directional couplers, Branch line Couplers, Design and Fabrication of Lumped elements for MICs, Comparison with distributed circuits.

UNIT – III NON-RECEPROCAL COMPONENTS AND ACTIVE DEVICES FOR MICS 9 Hrs

Ferromagnetic substrates and inserts, Micro strip circulators, Phase shifters, Microwave transistors, Parametric diodes and Amplifiers, PIN diodes, Transferred electron devices, UIMPATT, BARITT, Avalanche diodes, Microwave transistors circuits

UNIT – IV MICROSTRIP CIRCUIT DESIGN AND APPLICATIONS 9 Hrs

Introduction, Impedance transformers, Filters, High power circuits, Low power Circuits, MICs in satellite and Radar

UNIT –V MMIC TECHNOLOGY 9 Hrs

Fabrication process of MMIC, Hybrid MICs, Configuration, Dielectric substances, Thick and thin film technology, Testing methods, Encapsulation and mounting of Devices.

Total No. of Periods: 45

References:

1. Hoffman R.K. "*Handbook of Microwave integrated circuits*", Artech House, Boston, 1989
2. Gupta .K.C and Amarjit Singh, "*Microwave integrated circuits*" John Wiley, New York, 1975.

MEC13C008 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN 3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts of EMI design, measurements and control techniques

UNIT –I EMI ENVIRONMENT 9 Hrs

Sources of EMI conducted and radiated EMI, Transient EMI, EMI-EMC definitions and units of parameters. Emi Coupling Principles Conducted, Radiated and Transient Coupling, Common impedance Ground Coupling, Radiated Common Mode and Ground Loop coupling, Radiated Differential Mode Coupling, Near Field Cable to cable coupling, Power mains and Power supply Coupling.

UNIT –II EMI SPECIFICATION / STANDARDS / LIMITS 9 Hrs

Units of specification, Civilian standards Military standards, National and Intentional standardizing organizations- FCC, CISPR, ANSI, DOD, IEC, CENEEC, FCC CE and RE standards, CISPR, CE and RE Standards, IEC/EN, CS standards, Frequency assignment - spectrum conversation

UNIT –III EMI MEASUREMENTS 9 Hrs

EMI Test Instruments Systems, EMI Test, EMI shielded Chamber, Open Area Test Site, TEM Cell Antennas, Conductors Sensors / Injectors / Couplers,. Military Test Method and Procedures, Calibration Procedures.

UNIT –IV EMI CONTROL TECHINQUES 9 Hrs

Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting.

UNIT –V EMI DESIGN OF PCBs 9 Hrs

PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning Motherboard Design and Propagation Delay Performance Models.

Total Number of Periods: 45

References:

1. Bernhard Keiser, "*Principles of Electromagnetic compatibility*", Artech House, #rd Ed, 1986.
2. Henry W. Ott, "*Noise Reduction Techniques in Electronic Systems*", John Wiley and Sons, New York, 1988.
3. V.P. Kodali, "*Engineering EMC Principles, Measurements and Technologies*", IEEE Press, 1996.
4. Clayton R. Paul – *"Introduction to Electromagnetic compatibility*" – Wiley & Sons – 1992

MEC13CE01 MULTIMEDIA COMPRESSION TECHNIQUES 3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts of audio, video, image and text compression.

UNIT – I INTRODUCTION 9 Hrs

Brief history of data compression applications, Overview of information theory, redundancy.Overview of Human audio, visual systems, Taxonomy of compression techniques. Overview of source coding, Source models, Scalar quantisation theory, Rate distribution theory, Vector quantisation, Structure quantizers, Evaluation techniques-error analysis and methodologies.

UNIT – II TEXT COMPRESSION 9 Hrs

Compact techniques- Huffman coding – Arithmetic coding – Shannon Fano Coding and dictionary techniques – LZW family algorithms. Entropy measures of performance – Quality measures.

UNIT – III AUDIO COMPRESSION 9 Hrs

Audio compression techniques-Frequency domain and filtering-basic sub band coding-Application to speech coding-G.722-Application to audio coding-MPEG audio, Progressive encoding for audio—silence compression, Speech compression techniques-Vocoders

UNIT – IV IMAGE COMPRESSION 9 Hrs

Predictive techniques-PCM, DPCM, and DM. Contour based compression- quadtrees, EPIC, SPIHT, Transform coding PEG, JPEG-2000, and JBIG

UNIT – V VIDEO COMPRESSION 9 Hrs

Video signal representation, Video compression techniques-MPEG, Motion estimation techniques-H.261.Overview of Wavelet based compression and DVI technology, Motion video compression, PLV Performance, DVI real time compression

Total No of periods: 45

References:

1. Mark Nelson, "*Data Compression book*", BPB Publishers, New Delhi, 1998.
2. Sayood Khaleed, *Introduction to Data Compression*, Morgan Kauffman, London, 1995.
3. Warkinson, J."*Compression in video and audio*", Facol press, London. 1995
4. Jan Vozer, "*Video compression for multimedia*", AP profess, Newyork, 1995

MEC13C003 OPTICAL COMMUNICATION SYSTEMS AND NETWORKS

3 0 0 3

OBJECTIVES

- To enable the students to equip with the design issues of fiber optic systems

UNIT –I FIBRE OPTIC GUIDES **9 Hrs**

Light wave generation systems, systems components, optical fibers, SI, GI fiber, modes, Dispersion in fibers, Limitations due to dispersions, fiber loss, non liner effects

UNIT –II OPTICAL TRANSMITTERS AND FIBRES **9 Hrs**

Basic concepts, LED structures spectral distribution, Semiconductor lasers, Gain co-efficient, modes, SLM and STM operation, Transmitter design, Receiver PIN and APD diodes design, Noise sensitivity degradation,

UNIT –III LIGHT WAVE SYSTEM **9 Hrs**

Coherent, Homodyne and Hetero dyne keying formats, BER in synchronous and Asynchronous, WDM concepts, Key elements of optical fiber systems, Spectral bands, Standard for optical fiber communications.

UNIT – IV AMPLIFIERS **9 Hrs**

Basic concepts, Semiconductor laser amplifiers Raman-and Brillouin-fibre amplifiers, Erbium doped-fiber and amplifiers, pumping phenomenon

UNIT – V DISPERSION COMPENSATION **9 Hrs**

Limitations, Post-and pre-compensation techniques, Equalizing filters, Optical phase conjugation, fiber Bragg gratings, Channels at high bit rates, Electronic dispersion compensation.

Total No. of periods: 45

References:

1. Franze & Jain, "*Optical communication, systems and components*", Narosa Publication, New Delhi, 2000
2. G. Keiser, "*Optical fiber communication system*", McGraw Hill, Newyork, 2000
3. G.P Agarwal, "*Fiber optic communication system*". 2nd Edition, John Wiley & Sons, New York, 1997.
4. Franz and Jain, "*Optical communication system*", Narosa Publications, New Delhi, 1995

MEC13CE05 HIGH SPEED SWITCHING ARCHITECTURE 3 0 0 3

OBJECTIVES

- To equip the students with the concepts of high speed switching techniques in ATM networks.

UNIT – I HIGH SPEED NETWORK 9 Hrs

Introduction-LAN, WAN, Network evolution through ISDN to B-isdn, Transfer mode and control of B-ISDN, SDH multiplexing structure, ATM standard, ATM Adaption layers

UNIT – II LAN SWITCHING TECHNOLOGY 9 Hrs

Switching concepts, Switch forwarding techniques, Switch path control, LAB switching, cut through forwarding, Store and forward, Virtual LANS

UNIT –III ATM SWITCHING ARCHITECTURE 9 Hrs

Switch models, blocking networks-Basic-and-enhanced banyan networks, sorting networks-merge sorting, Re-arranegable networks-full-and-partial connection networks, Non-blocking networks-Recursive network construction, comparison of non-blocking network, Switches with deflection routing-shuffle switch, Tandem banyan

UNIT –IV QUEUES IN ATM SWITCHES 9 Hrs

Internal Queuing-Input, Output and shared queuing multiple queuing networks-
Combined input, Output and shared queuing-performance analysis of Queued Switches

UNIT – V IP SWITCHING 9 Hrs

Addressing model, IP Switching types-flow driven and topology driven solutions, IP over ATM address and next hop resolution, Multicasting, Ipv6 over ATM

Total No. of periods: 45

References:

1. Ranier Handel, Manfred N Huber, Stefan Schroder, "*ATM Networks- concepts protocols applications*", 3rd Edition, Addison Wesley, New York, 1999
2. Achille Pattavina, "*Switching Theory: Architecture and performance in broadband ATM Networks*", John Wiley & Sons Ltd., New York. 1998
3. Christopher Y Metz, "*Switching protocols & Architectures*", McGraw Hill Professionals Publishing, NewYork.1998.

MEC13AE03 SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS 3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts of optimization of digital circuits with various algorithms.

UNIT-I CIRCUITS AND HARDWARE MODELING 9 Hrs

Design of Microelectronic Circuits - Computer Aided Synthesis and optimization Graph – Optimization, problems and algorithms-Combinatorial optimization-Boolean Algebra and Application -Hardware Modeling, Languages – Compilation and Behavioral optimization**.**

UNIT-II ARCHITECTURAL LEVEL SYNTHESIS AND OPTIMIZATION. 9 Hrs

Circuit specification for Architectural synthesis -Fundamental Architectural synthesis Problems-Area and performance Estimation-Control unit synthesis-synthesis of pipelined circuits**.**

UNIT-III SCHEDULING ALGORITHMS AND RESOURCE SHARING. 9 Hrs

Unconstrained Scheduling -ASAP Algorithm-ALAP Scheduling Algorithm - Scheduling with Resource Constraints-Scheduling pipelined circuits -Sharing and binding for Dominated circuits -Area Binding-Concurrent Binding –Module selection problems -Structural testability.

UNIT-IV LOGIC-LEVEL SYNTHESIS AND OPTIMIZATION 9 Hrs

Logic optimization Principles-Algorithms and logic Minimization –Encoding problems- Multiple-level optimization of logic networks -Algebraic and Boolean model -Algorithm for delay Evaluation -Rule based logic optimization.

UNIT-V CELL-LIBRARY BINDING AND STATE OF ART IN SYNTHESIS 9 Hrs

Specific problem and algorithm for library Binding – Structural matching - Boolean matching- concurrent, logic optimization and library binding - Production level synthesis systems, Research synthesis systems -System level synthesis, Hardware soft ware co-design.

Total No. of periods: 45

References:

1. Giovanni De Micheli, "*Synthesis and optimization of Digital Circuits*", Tata McGraw -Hill, 2003.
2. John Paul Shen, Mikko H. Lipasti, "*Modern processor Design*", Tata McGraw Hill, 2003

MEC13VE03 EMBEDDED LINUX 3 0 0 3

OBJECTIVES

- To enable the students to understand the concepts of Embedded Linux basics and their applications

UNIT –I FUNDAMENTALS OF OPERATING SYSTEMS 8 Hrs

Overview of operating systems – Process and threads – Processes and Programs – Programmer view of processes – OS View of processes – Threads - Scheduling – Non pre-emptive and pre-emptive scheduling – Real Time Scheduling – Process Synchronization – Semaphores – Message Passing – Mailboxes – Deadlocks – Synchronization and scheduling in multiprocessor Operating Systems

UNIT – II LINUX FUNDAMENTALS 10 Hrs

Introduction to Linux – Basic Linux commands and concepts – Logging in - Shells - Basic text editing - Advanced shells and shell scripting – Linux File System –Linux programming - Processes and threads in Linux - Inter process communication – Devices – Linux System calls

UNIT –III INTRODUCTION TO EMBEDDED LINUX 8 Hrs

Embedded Linux – Introduction – Advantages- Embedded Linux Distributions - Architecture - Linux kernel architecture - User space – Linux startup sequence - GNU cross platform Tool chain.

UNIT – IV BOARD SUPPORT PACKAGE AND EMBEDDED STORAGE 10 Hrs

Inclusion of BSP in kernel build procedure - The boot loader Interface – Memory Map – Interrupt Management – PCI Subsystem – Timers – UART – Power Management – Embedded Storage – Flash Map – Memory Technology Device (MTD) –MTD Architecture - MTD Driver for NOR Flash – The Flash Mapping drivers – MTD Block and character devices – mtdutils package – Embedded File Systems – Optimizing storage space – Turning kernel memory.

UNIT – V EMBEDDED DRIVERS AND APPLICATION PORTING 9 Hrs

Linux serial driver – Ethernet driver – I2C subsystem – USB gadgets – Watchdog timer – Kernel Modules – Application porting roadmap - Programming with pthreads – Operating System Porting Layer – Kernel API Driver - Case studies - RT Linux – uC Linux

Total No. of Hrs: 45

References:

1. Dhananjay M. Dhamdhere, "*Operating Systems A concept based Approach*", Tata McGraw-Hill Publishing Company Ltd
2. Matthias Kalle Dalheimer, Matt Welsh, "*Running Linux*", O'Reilly Publications 2005
3. Mark Mitchell, Jeffrey Oldham and Alex Samuel "*Advanced Linux Programming*" New Riders Publications
4. P. Raghavan , Amol Lad , Sriram Neelakandan, "*Embedded Linux System Design and Development*", Auerbach Publications 2006
5. Karim Yaghmour, "*Building Embedded Linux Systems*", O'Reilly Publications 2003