Dr. M.G.R.
EDUCATIONAL AND RESEARCH INSTITUTE
UNIVERSITY
(Decl. U/S 3 of the UGC Act 1956)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M. TechVLSI Design and Embedded System
CURRICULUM AND SYLLABUS (Part Time)
2013 REGULATION

I SEMESTER						
S.No	**Subject Code**	**Title of the Subject**	**L**	**T**	**P**	**C**
1	MMA130006	Applied Mathematics for Electronics Engineers	3	1	0	4
2	MEC13A003	Advanced Digital System Design	3	0	0	3
3	MEC13A001	Advanced Digital Signal Processing	3	0	0	3
		Total	**9**	**1**	**0**	**10**

II SEMESTER						
S.No	**Subject Code**	**Title of the Subject**	**L**	**T**	**P**	**C**
1	MEC13V001	VLSI Architecture and Design Methodologies	3	1	0	4
2	MEC13A004	Microcontroller Based System Design	3	0	0	3
3	MEC13V002	Real-time Operating Systems and System programming using C/C++	3	0	0	3
4	MEC13VL01	VLSI Design Lab	0	0	3	2
		Total	**9**	**1**	**3**	**12**

III SEMESTER						
S.No	**Subject Code**	**Title of the Subject**	**L**	**T**	**P**	**C**
1	MEC13V004	VLSI Signal Processing	3	0	0	3
2	MEC13V006	VLSI for Wireless Communication	3	0	0	3
3	MEC13V007	DSP Architecture	3	1	0	4
		Total	**9**	**1**	**0**	**10**

IV SEMESTER						
S.No	**Subject Code**	**Title of the Subject**	**L**	**T**	**P**	**C**
1	MEC13V008	Computer Aided Design of VLSI Circuits	3	0	0	3
2	MEC13V009	Electronic Design Automation Tools	3	1	0	4
3	MEC13V010	Embedded System Design	3	0	0	3
4	MEC13VL02	Embedded System Design Lab	0	0	3	2
		Total	**9**	**1**	**4**	**12**

V SEMESTER						
S.No	**Subject Code**	**Title of the Subject**	**L**	**T**	**P**	**C**
1	MEC13V011	VLSI Testing and Verification	3	1	0	4
2	MEC13V012	ASIC Design	3	1	0	4
3	MEC13VEXX	Elective – I	3	0	0	3
4	MEC13VL03	Project Phase – I	0	0	5	5
		Total	**9**	**2**	**5**	**16**

VI SEMESTER						
S.No	**Subject Code**	**Title of the Subject**	**L**	**T**	**P**	**C**
1	MEC13VL04	Project Work & Viva Voce	0	0	24	15
		Total	**0**	**0**	**24**	**15**

Total Credits: 75

ELECTIVES						
S.No	**Subject Code**	**Title of the Subject**	**L**	**T**	**P**	**C**
1	MEC13VE01	VLSI Technology	3	0	0	3
2	MEC13VE02	Optimization Techniques and Their applications in VLSI Design	3	0	0	3
3	MEC13VE03	Embedded Linux	3	0	0	3
4	MEC13VE04	Introduction to MEMS System Design	3	0	0	3
5	MEC13VE05	Embedded Networking	3	0	0	3
6	MEC13A006	Computer Architecture and Parallel Processing	3	0	0	3
7	MEC13VE06	Design of Embedded Control System	3	0	0	3
8	MEC13VE07	Advanced Embedded Systems	3	0	0	3
9	MEC13VE08	Distributed Embedded Computing	3	0	0	3

MMA130006 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS 3 1 0 4

OBJECTIVES

- To enable the students to learn the basic concepts of random process and special functions

UNIT – I ADVANCED MATRIX THEORY 12 Hrs

Generalized Eigen vectors-Jordan canonical form –Matrix Norms-QR algorithm-Pseudo Inverse-Singular value decomposition –Least Square Solutions.

UNIT – II RANDOM PROCESS 12 Hrs

Classification of Random Process-Stationary Process-Ergodic Process-Markov Process –Markov Chains-Auto Correlation –Auto Covariance –Cross Correlation-Cross Covariance-Spectral Density.

UNIT – III SPECIAL FUNCTIONS 12 Hrs

Bessel's Equation-Bessel Functions-Recurrence relations-Generating function-Orthogonal property-Legendre's equation-Legendre Polynomials- Rodrigue's formula.

UNIT – IV CALCULUS OF VARIATIONS 12 Hrs

Variation and its properties-Euler's equations- Functional dependent on First and Higher Order Derivatives-Functional depend on functions of several independent variables-Problems with moving boundaries-Direct methods-Ritz and Kantorovich methods.

UNIT – V INTEGRAL EQUATIONS 12 Hrs

Types of Integral equations-Fredholm Integral equation-Volteera Integral equation-Green's function- Fredholm Integral equations with Separable kernels- Iterative methods solving equations of second kind- Properties of Symmetric kernels.

Total No. of Hours: 60

Reference Books:

1. Bronson R., "*Theory and problems of Matrix Operations"* (Schaum's Outline Series), Mc Graw Hill, (1989)
2. Lewis D.W., *"Matrix theory"*, Allied publishers,(1995)
3. Richard Johnson A., *"Miller & Freund's Probability and Statistics for Engineers"* (8th Ed.) Prentice Hall of India(2009)
4. Veerarajan T., *"Probability Statistics and Random Process"* , Tata McGraw Hill Publishing Co.,(2008)
5. Venkataraman M.K., " *Higher Mathematics for Engineering and Science"* , The National Publishing Co.,(2006)
6. Gupta A.S., *"Calculus of variations with applications"*, Prentice Hall of India,(2004)
7. Raisinghania M.D., *"Integral Equations and Boundary Value Problems"* (3rd ed), S. Chand & Co., (2010)
8. Hildebrand F.B., *"Methods of Applied Mathematics*" , Dover Books,(1992)

MEC13A003 ADVANCED DIGITAL SYSTEM DESIGN 3 0 0 3

OBJECTIVES

- To enable the students the ability to design complex sequential circuits
- To equip the students with the ability to detect and correct faults using various algorithms

UNIT I SEQUENTIAL CIRCUIT DESIGN 9 Hrs

Analysis of Clocked Synchronous Sequential Networks (CSSN), Modeling of CSSN, State Stable Assignment and Reduction, Design of CSSN, Design of Iterative Circuits, ASM Chart, ASM Realization, Design of Arithmetic circuits for Fast adder- Array Multiplier.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9 Hrs

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9 Hrs

Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9 Hrs

Programming Techniques -Re-Programmable Devices Architecture- Function blocks, I/O blocks, Interconnects, Realize combinational, Arithmetic, Sequential Circuit with Programmable Array Logic; Architecture and application of Field Programmable Logic Sequence.

UNIT V NEW GENERATION PROGRAMMABLE LOGIC DEVICES 9 Hrs

Fold back Architecture with GAL, EPLD, EPLA , PEEL, PML; PROM – Realization State Machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 - Xilinx 3000

Total No. of Hrs: 45

References:

1. Donald G. Givone, "*Digital Principles and Design*", Tata McGraw Hill 2002.
2. Stephen Brown and ZvonkVranesic, "*Fundamentals of Digital Logic with VHDL Design*", Tata McGraw Hill, 2002
3. Mark Zwolinski, "*Digital System Design with VHDL*", Pearson Education, 2004
4. Parag K Lala, "*Digital System design using PLD*", BS Publications, 2003
5. John M Yarbrough, "*Digital Logic Applications and Design*", Thomson Learning, 2001
6. Nripendra N Biwa's, "*Logic Design Theory*", Prentice Hall of India, 2001
7. Charles H. Roth Jr., "*Fundamentals of Logic Design*", Thomson Learning, 2004.

MEC13A001 ADVANCED DIGITAL SIGNAL PROCESSING 3 0 0 3

OBJECTIVES

- To enable the students to get the fundamentals of parametric and non-parametric analysis
- To enable the students to design adaptive filters using different methodologies

UNIT -I DISCRETE RANDOM SIGNAL PROCESSING 9 Hrs

Discrete Random Process, Expectation, Variance, Co-Variance, Scalar Product, Energy of Discrete Signal-Parseval's Theorem, Wiener Khintchine Relation-Power Spectral Density –Periodogram – Sample Autocorrelation-Sum Decomposition Theorem, Spectral Factorization Theorem – Discrete Random Signal Processing by Linear Systems-Simulation of White Noise – Low Pass Filtering of White Noise.

UNIT - II SPECTRUM ESTIMATION 9 Hrs

Non-Parametric Methods-Correlation Method – Co-Variance Estimator – Performance Analysis of Estimators – Unbiased, Consistent Estimators – Periodogram Estimator – Barlett Spectrum Estimation – Welch Estimation – Model based Approach – AR, MA, and ARMA Signal Modeling – Parameter Estimation using Yule-Walker Method.

UNIT - III LINEAR ESTIMATION AND PREDICTION 9 Hrs

Maximum likelihood criterion-efficiency f estimator – Least mean squared error criterion – Wiener filter – Discrete Wiener Hoff equations – Recursive estimators-Kalman filter – Linear prediction, prediction error-whitening filter, inverse filter – Levinson recursion, Lattice realization, and Levinson recursion algorithm for solving Teoplitz system of equations.

UNIT -IV ADAPTIVE FILTERS 9 Hrs

FIR adaptive filters – Newton's steepest descent method-adaptive filter based on steepest descent method – Widrow Hoff LMS adaptive algorithm – Adaptive channel equalizations – Adaptive echo chancellor – Adaptive noise cancellation – RLS adaptive filters –Exponentially weighted RLS – sliding window RLS – Simplified IIR LMs adaptive filter

UNIT – V MULTIRATE DIGITAL SIGNAL PROCESSING 9 Hrs

Mathematical description of change of sampling rate – Interpolation and Decimation –continuous time model – Direct digital domain approach -Decimation by an integer factor – Interpolation by an integer factor – single and multistage realization - Poly phase realization – Application to sub band coding – Wavelet transform and filter bank implementation of wavelet expansion of signals.

Total No. of Hrs: 45

References:

1. Monson H. Hayes, "*Statistical Digital Signal Processing and Modeling*", John Wiley and Sons, Inc., New York, 1996
2. Sopocles J. Orfanidis, "*Optimum Signal Processing*", McGraw Hill, 1990.
3. John G. Proakis, Dimitris G. Manolakis, "*Digital Signal Processing*", Prentice Hall of India, 1995

MEC13V001 VLSI ARCHITECTURE AND DESIGN METHODOLOGIES 3 1 0 4

OBJECTIVES

- To enable the students to absorb the concepts of different PLDs
- To enable the students to equip with the different ASIC and FPGA Techniques

UNIT I CMOS DESIGN 12 Hrs

Overview of digital VLSI design Methodologies- Logic design with CMOS-transmission gate circuits-Clocked CMOS-dynamic CMOS circuits, Bi-CMOS circuits- Layout diagram, Stick diagram-IC fabrications – Trends in IC technology.

UNIT II PROGRAMABLE LOGIC DEVICES 12 Hrs

Programming Techniques-Anti fuse-SRAM-EPROM and EEPROM technology –Re-Programmable Devices Architecture- Function blocks, I/O blocks, Interconnects, Xilinx- XC9500,Cool Runner - XC-4000,XC5200, SPARTAN, Virtex - Altera MAX 7000- Flex 10K-Stratix.

UNIT III ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT & ROUTING 12 Hrs

System partition – FPGA partitioning – Partitioning methods- floor planning – placement physical design flow – global routing – detailed routing – special routing- circuit extraction – DRC.

UNIT IV ANALOG VLSI DESIGN 12 Hrs

Introduction to analog VLSI- Design of CMOS 2stage-3 stage Op-Amp –High Speed and High frequency op-amps-Super MOS-Analog primitive cells-realization of neural networks.

UNIT V LOGIC SYNTHESIS AND SIMULATION 12 Hrs

Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioural modelling, task & functions, Verilog and logic synthesis-simulation-Design examples, Ripple carry Adders, Carry Look ahead adders, Multiplier, ALU, Shift Registers, Multiplexer, Comparator, Test Bench.

Total Hrs: 60

References:

1. M.J.S Smith, "*Application Specific Integrated Circuits*", Addition Wesley LongmanInc.1997.
2. Kamran Eshraghian, "*Douglas A. Pucknell and Sholeh Eshraghian,"Essentials of VLSI circuits and System"*, Prentice Hall India, 2005.
3. Wayne Wolf, *"Modern VLSI Design*" Prentice Hall India, 2006.
4. Mohamed Ismail, Terri Fiez, "*Analog VLSI Signal and Information Processing*", McGraw Hill International Editions, 1994.
5. Samir Palnitkar, "*Verilog HDL, A Design Guide to Digital and Synthesis*" 2nd Ed, Pearson, 2005.

MEC13A004 MICROCONTROLLER BASED SYSTEM DESIGN 3 0 0 3

OBJECTIVES

- To enable the students to design microcontroller based embedded systems
- To enable the students to develop real-time peripheral applications

UNIT – I 8051 MICROCONTROLLER 9 Hrs

Intel 8051 Architecture – Hardware – I/O ports – External Memory – Counters and Timer – Serial data I/O – Interrupts, Assembly language, Addressing modes, Instruction Set - Simple programs, 8051 interfacing to LCD, ADC, DAC and Stepper Motors.

UNIT- II 68HC11 MICROCONTROLLER 9 Hrs

Motorola 68HC11 Architecture – Input / Output ports – Resets and self protection – Interrupt Timing – A/D D/A converters.

UNIT – III 8096 MICROCONTROLLER 9 Hrs

Intel 8096 CPU Structure, programming structure – Register file – Assembly Language – Addressing modes – Instruction set – simple programs.

UNIT -IV PIC MICROCONTROLLER 9 Hrs

Architecture – memory organization – addressing modes – instruction set – PIC programming in Assembly & C – I/O port, Data Conversion, RAM & ROM Allocation, Timer programming, MP-LAB.

UNIT- V PERIPHEREL OF PIC MICROCONTROLLER 9 Hrs

Timers – Interrupts, I/O ports- I2C bus-A/D converter-UART- CCP modules -ADC, DAC and Sensor Interfacing – Flash and EEPROM memories.

Total No. of Hours: 45

References:

1. Kenneth J. Ayala, "*The 8051 Microcontroller Architecture, Programming & Applications*" – Penram International publishing (India), Second Edition, 1996.
2. Muhammed Ali Mazidi, Janice Gillies Pie Mazidi, "*The 8051 Microcontroller and Embedded Systems*"– Pearson Education Asia.
3. PEATMAN J.B, "*Design with Microcontrollers*" – McGraw Hill Book International Ltd, Singapore, 1989.
4. John Iovine, "*PIC Microcontroller Project Book*", McGraw Hill 2000
5. Myke Predko, "*Programming and Customizing the 8051 Microcontroller*", Tata McGraw Hill 2001

MEC13V002REAL-TIME OPERATING SYSTEMS &SYSTEM PROGRAMMING USING C/C++ 300 3

OBJECTIVES

- To enable the students to develop real-time applications using various architectures and scheduling algorithms
- To enable the students to solve real-time issues with embedded tools

UNIT- I EMBEDDED SYSTEM FUNDAMENTALS 9 Hrs

Introduction, Characteristics of embedded systems and challenges in system design –Design issues in embedded real-time systems, Critical performance issues in embedded real-time systems. Software builds process- infinite loop process, compiling, linking & locating. Software porting issues on target hardware, Code optimization

UNIT - II SURVEY OF SOFTWARE ARCHITECTURES 9 Hrs

Round –robin, Round-robin with interrupts, Queues. Function- scheduling architecture, Real time operating system architecture, Scheduling architecture.

UNIT- III ELEMENTS OF REAL TIME OPERATING SYSTEMS 9 Hrs

Tasks & task states, tasks & data, semaphores & shares data, message queues, mailboxes and pipes, Timer functions, Events, Memory management and interrupt routines in an RTOS environment.

UNIT –IV BASIC DESIGN USING REAL-TIME OPERATING SYSTEMS 9 Hrs

Principles, Encapsulating semaphores & queues, hard real-time scheduling considerations, saving memory space, saving power.

UNIT- V EMBEDDED TOOLS 9 Hrs

Embedded software development tools- host and target machines, Linker/locators for embedded software, getting embedded software into the target system. Debugging techniques- testing on host system, Instruction set simulators, the assert, Macro using laboratory tools

Total No. of Hrs: 45

References:

1. David e. Simon, "*An Embedded Software Primer*", Pearson education, 1999.
2. Arnold s. Berger, "*Embedded Systems Design- An Introduction to Processes, Tools &Techniques"*, CMP books, 2002.
3. Jean j. Labrosse, "*Embedded Systems Building Blocks*", CMP books, 2002.
4. Michael Barr, "*Programming Embedded Systems in C and C++*", O'Reilly, 1999.
5. Wayne wolf, "*Computers as Components- Principles of Embedded Computing Systems Design"*, academic press, 2001.

MEC13VL01 **VLSI DESIGN LAB** **0 0 3 2**

OBJECTIVES

- To enable the students to design digital systems using PIC microcontroller, EDA tools like VHDL and Verilog

1. DESIGN USING PIC MICROCONTROLLER.

2. IMPLEMENTATION OF ADAPTIVE FILTERS-PERIODOGRAM AND MULTISTAGE MULTIRATE SYSTEM IN DSP PROCESSOR.

3. ANALYSIS OF MULTIRATE SIGNALS USING SIMULATION PACKAGES.

4. MODELING OF SEQUENTIAL DIGITAL SYSTEM USING VHDL.

5. MODELING OF SEQUENTIAL DIGITAL SYSTEM USING VERILOG.

6. DESIGN AND IMPLEMENTATION OF ALU USING FPGA.

7. SIMULATION OF NMOS AND CMOS CIRCUITS USING SPICE.

MEC13V006 VLSI FOR WIRELESS COMMUNICATION 3 0 0 3

OBJECTIVES

- To learn the performance of different A-D Convertors and coding techniques like LDPC and convolution codes.
- To learn the basics of OFDM technique and its performance metrics and various transceiver architecture for modern wireless communication system.

UNIT-I ANALOG TO DIGITAL CONVERSION 9 Hrs

Performance metrics for Analog-to-digital converters, Sampling, Band-pass Sampling, Quantization, Types of Analog-to-digital converters, Sigma Delta Analog-to-digital converters.

UNIT -II CODING THEORY ALGORITHM AND ARCHITECTURE 9 Hrs

Convolution codes, trellis diagram, Viterbi algorithm, Soft input decoding, soft output decoding, Turbo codes, LDPC coding, Concatenated convolution codes, weight distribution, Space-Time codes, Spatial channels, Performance measure, Orthogonal space-time block codes, Spatial multiplexing.

UNIT- III TRANSCIEVER ARCHITECTURE AND ISSUES 9 Hrs

Receiver Architectures, Super heterodyne receiver, Image rejection receiver,-Hartley and Weaver, Zero IF receiver, Low IF receiver, Transmitter architecture, Super heterodyne transmitter, Direct up transmitter, Two-step-up transmitter, Transceiver architectures for modern wireless systems, Case study.

UNIT- IV OFDM SYSTEM 9 Hrs

Principle, propagation characteristics, principle, mathematical model, OFDM baseband signal processing, Receiver design, Automatic gain control and DC offset compensation, code sign of Automatic gain control and timing synchronization, code sign of filtering and timing synchronization, Transmit chain setup.

UNIT- VANALOG IMPAIRMENT AND ISSUES 9 Hrs

Receiver sensitivity and noise figure, DC offsets, LO leakage, Receiver interferers and inter-modulation distortion, Image rejection, Quadrature balance and relation to Image rejection, relation to EVM, Peak to average power ratio , Local oscillator pulling in PLL, effect of phase noise in PLL, Effect of phase noise on OFDM systems, Effect of frequency errors on OFDM systems.

Total No. of Hrs: 45

References:

1. Pui-In Mak, Seng-Pan U, Rui Paulo Martins, "*Analog-Baseband Architectures and Circuits for Multi standard and Low Voltage Wireless Transceivers*", springer, 2007.
2. Emad N. Farag, Mohamed I. Elmasry, "*Mixed signal VLSI Wireless Design Circuits and Systems*", Kluwer Academic Publishers, 2002.
3. Andre Neubauer, Jurgen Freudenberger, Volker Kuhn, *"Coding theory, Algorithms, Architectures and Applications*", John Wiley & Sons, 2007.
4. Wolfgang Eberle, "*Wireless Transceiver Systems Design*", Springer, 2008.

MEC13V004 VLSI SIGNAL PROCESSING 3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts of parallel processing, pipelining and various fast convolution techniques

UNIT - I PIPELINING AND PARALLEL PROCESSING 8 Hrs

Introduction - Pipelining of FIR Digital filters - Parallel processing - Pipelining and parallel processing for Low power.

UNIT - II RETIMIMG 12 Hrs

Introduction - Definitions and Properties - Solving system of Inequalities - Retiming Techniques. Folding: - An algorithm for unfolding - Properties of unfolding - Critical path, unfolding and retiming - Application of unfolding.

UNIT – III SYSTOLIC ARCHITECTURE DESIGN 9 Hrs

Introduction - systolic Array Design Methodology - FIR systolic Arrays - Selection of scheduling vector - Matrix Multiplication and 2D systolic array Design - Systolic design for space representations containing Delays .

UNIT -IV FAST CONVOLUTION 8 Hrs

Introduction -Cook -Toom algorithm - Winograd algorithm - Iterated convolution - cyclic Convolution - Design of Fast convolution -Algorithm by Inspection.

UNIT – V SCALING AND ROUNDOFF NOISE 8 Hrs

Introduction – Scaling and Round off noise – State variable Description of digital filters – Scaling and Round off noise computation – Round off Noise in Pipelined IIR filter – Round off Noise Computation Using State variable description – Slow down, retiming, and pipelining.

Total No. of Hrs: 45

References:

1. Keshab. K. Parhi, "*VLSI Digital Signal Processing Systems-Design and Implementations"*, Wiley - Inter science, 1999.
2. Mohammed Ismail, Terri, Fiez, "*Analog VLSI Signal and Information Processing*", 1994 McGraw Hill.
3. Kung .S.Y, H.J. While house, T. Kailath, "*VLSI and Modern Signal Processing*", Prentice hall, 1985
4. Jose E. France, Yannis Tsividis "*Design of Analog - Digital VLSI Circuits for Telecommunications and Signal Processing"* - Prentice Hall, 1994.

MEC13V007 DSP ARCHITECTURE 3 1 0 4

OBJECTIVES

- To analyze and study different DSP architectures and their applications

UNIT – I INTRODUCTION TO DSP 12 Hrs

Introduction, A Digital Signal Processing systems, the sampling process, Discrete Time Sequences, DFT, and FFT, Linear Time Invariant Systems, Digital Filters, Decimation and Interpolation, Analysis and Design Tool for DSP Systems

UNIT–II ARCHITECTURES FOR PROGRAMMABLE DIGITAL SIGNAL PROCESSING DEVICES 12 Hrs

Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for external Interfacing

UNIT -III PROGRAMMABLE DIGITAL SIGNAL PROCESSORS 12 Hrs

Introduction, Commercial Digital signal processing devises, data addressing modes of TMS 320C54xx digital signal processors, Memory space of TMS 320C54xx processors, Program control, TMS 320C54xx Instructions and Programming, On chip peripherals, Interrupts of TMS 320C54xx processors, Pipeline operation of TMS 320C54xx processors

UNIT –IV INTERFACING TO PROGRAMMABLE DSP DEVICE 12 Hrs

Introduction, memory space organization, external bus interfacing signals, memory interface, parallel I/O interface, programmed I/O, interrupts and I/O, direct Memory Access (DMA) ,Synchronous serial interface, a multi channel buffered serial port, (McBSP), McBSP Programming, A CODEC interface circuit, CODEC Programming, A CODEC-DSP interface example

UNIT –V APPLICATIONS OF PROGRAMMABLE DSP DEVICES 12 Hrs

Introduction to DSP system, DSP Based Bio-telemetry receiver, a speech processing system, an image processing system-compression and transmission, radar signal processing, Telecommunications-wireless network.

Total No. of Hrs: 60

References:

1. "*Digital Signal Processing*", by Avatar Singh and S Srinivasan 2004 (Thomson Learning)
2. "*Digital Signal Processing*", A Practical Approach by Fletcher E.C., Jervis B.W. 2nd Edition 2002 (Pearson Education)
3. "*Digital Signal Processors"* by B Venkataramani and M Bhaskar 2002 (TMH)

MEC13V008 COMPUTER AIDED DESIGN OF VLSI CIRCUITS 3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts of different VLSI physical design automation tools

UNIT – I VLSI Physical Design Automation **9 Hrs**

VLSI Methodologies – VLSI Physical Design Automation – Design and Fabrication of VLSI Devices – Fabrication process and its impact on Physical Design.

UNIT – II Algorithms and Graph Theory **9 Hrs**

VLSI Design Automation Tools - Data structures and Basic Algorithms – Algorithms Graph Theory and computational complexity – Tractable and Intractable problems

UNIT – III Partitioning – Floor planning **9 Hrs**

General purpose methods for combinational optimization – Partitioning – Floor planning and pin assignment – placement

UNIT – IV Routing and High-level Synthesis **9 Hrs**

Simulation – Logic synthesis – Verification – High-level synthesis – compaction, Routing: detailed routing, global routing

UNIT – V VHDL and Verilog Implementation **9 Hrs**

Physical Design Automation of FPGAs, MCMS – VHDL – Verilog - Implementation of simple circuits using VHDL and Verilog packaging

Total No. of Hrs: 45

References:

1. N.A. Sherwani, "*Algorithms for VLSI Physical Design Automation*". 1999.
2. S.H. Gerez, "*Algorithms for VLSI Design Automation*", 1998.

MEC13V009 ELECTRONIC DESIGN AUTOMATION TOOLS 3 1 0 4

OBJECTIVES

- To enable the students to understand and analyze different EDA tools

UNIT 1 OS Overview 12 Hrs

An overview of OS commands. System settings and configuration. Introduction to Unix commands. Writing Shell scripts. VLSI design automation tools. An overview of the features of practical CAD tools.Modelsim, Leonardo spectrum, ISE 8.1i, Quartus II, VLSI backend tools.

UNIT II VHDL and Verilog Implementation 12 Hrs

Synthesis and simulation using HDLs-Logic synthesis using verilog and VHDL.Memory and FSM synthesis. Performance driven synthesis, Simulation- Types of simulation. Static timing analysis. Formal verification. Switch level and transistor level simulation.

UNIT II PSPICE Concepts 12 Hrs

Circuit simulation using Spice - circuit description.AC, DC and transient analysis. Advanced spice commands and analysis. Models for diodes, transistors and opamp.Digital building blocks. A/D, D/A and sample and hold circuits.

UNIT IV Mixed Signal Analysis 12 Hrs

Design and analysis of mixed signal circuits.Mixed signal circuit modeling and analysis using VHDL –AMS.

UNIT V System C 12 Hrs

System design using systemC- SystemC models of computation. Classical hardware modeling in system C. Functional modeling. Parameterized modules and channels. Test benches. Tracing and debugging.

Total No. of Hrs: 60

References:

1. M.J.S. Smith, "*Application Specific Integrated Circuits*",Pearson,2002
2. M.H. Rashid, "*Spice for Circuits and Electronics using Pspice*". (2/e), PHI.
3. T. Grdtker, "*System Design with C*", Kluwer, 2004.
4. P.J. Ashen den et al , "*The System Designer's Guide to VHDL-AMS*", Elsevier, 2005

MEC13V010 EMBEDDED SYSTEM DESIGN 3 0 0 3

OBJECTIVES

- To enable the students to basics of embedded processors and design systems using RISC processors

UNIT – I INTRODUCTION TO EMBEDDED PROCESSORS 9 Hrs

Embedded Computers, Characteristics of Embedded Computing Applications, and Challenges in Embedded Computing system design.Embedded system design process – Requirements, Specifications, Architecture Design, Designing hardware and software components, System integration.

UNIT –II EMBEDDED PROCESSOR & COMPUTING PLATFORM 9 Hrs

Data operations, Flow of control, SHARC processor – Memory organization, Data operations, Flow of control, Parallelism with instructions, CPU Bus Configuration, ARM Bus, SHARC bus, Memory devices, input/output devices, Component interfacing, Designing with microprocessor development and debugging.

UNIT – III PROGRAMMING EMBEDDED SYSTEMS 9 Hrs

Embedded Program – Role of Infinite loop – Compiling, Linking and locating – downloading and debugging – Emulators and simulators processor – External peripherals – Types of memory – Memory testing – Flash Memory.

UNIT – IV C ANDASSEMBLY 9 Hrs

Overview of Embedded C - Compilers and Optimization - Programming and Assembly – Register usage conventions – typical use of addressing options – instruction sequencing – procedure call and return – parameter passing – retrieving parameters – everything in pass by value – temporary variables.

UNIT–V EMBEDDED PROGRAM AND SOFTWARE DEVELOPMENT PROCESS 9 Hrs

Program Elements – Queues – Stack- List and ordered lists-Embedded programming in C++ - Inline Functions and Inline Assembly - Portability Issues - Embedded Java- Software Development process: Analysis – Design- Implementation – Testing – Validation- Debugging - Software maintenance.

Total No. of Hrs: 45

References:

1. W. Wolf, *"Computers as Components: Principles of Embedded Computing Systems Design*", Morgan Kaufman Publisher, 2001, ISBN 1-55860-541-x (case), ISBN 1-55860-693-9 (paper)
2. Daniel W. lewis "*Fundamentals of Embedded Software where C and Assembly meet*" PHI 2002.
3. Raj Kamal, "*Embedded Systems- Architecture, Programming and Design*" Tata McGraw Hill, 2006.
4. F. Wahid, "*Embedded System Design*" John Wiley & Sons publisher. ISBN – 13, 9789971514051, ISBN – 9971514052, (Paper)

MEC13VL02 EMBEDDED SYSTEM DESIGN LAB 0 0 3 2

OBJECTIVES

- To expose the students to different programming concepts in MATLAB and using ARM

1. Design with 8 bit Microcontrollers 8051/PIC Microcontrollers
   i) I/O Programming, Timers, Interrupts, Serial port programming
   ii) PWM Generation, Motor Control, ADC/DAC, LCD and RTC Interfacing, Sensor Interfacing
   iii) Both Assembly and C programming

2. Design with ARM Processors.
   I/O programming, ADC/DAC, Timers, Interrupts.

3. Study of one type of Real Time Operating Systems (RTOS)

4. Electronic Circuit Design of sequential, combinational digital circuits using CAD Tools

5. Simulation of digital controllers using MATLAB/Lab VIEW.

6. Programming with DSP processors for Correlation, Convolution, Arithmetic adder, Multiplier, Design of FIR&IIR Filters

7. Design with Programmable Logic Devices using Xilinx/Altera FPGA and CPLD

8. Design and Implementation of simple Combinational/Sequential Circuits

MEC13V011 VLSI TESTING &VERIFICATION 3 1 0 4

OBJECTIVES

- To enable the students to learn the concepts of hardware testing and fault debugging

UNIT – I INTRODUCTION TO TESTING 12 Hrs

Universal test. Pseudo-exhaustive and iterative logic array testing. Clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.

UNIT – II FAULT MODELING AND SIMULATION 12 Hrs

Faults and their manifestations. Fault models. Combinational logic and fault simulation. Test generation basics. Structural and non-structural test generation techniques. Combinational ATPG. Current sensing based testing.

UNIT – III TEST GENERATION 12 Hrs

Classification of sequential ATPG methods. Fault collapsing and simulation Test generation for synchronous and asynchronous circuits. Test compaction.

UNIT – IV ANALOG &MIXED SIGNAL TESTING 12 Hrs

Memory Test - Memory Test Levels, Memory Testing, Definitions, Static ADC and DAC Testing Methods.

UNIT – V DESIGN FOR TESTABILITY 12 Hrs

Design for testability: Scan design, use of scan chains, boundary scan. Built-in self test. Synthesis for testability.

Total No. of Hrs: 60

References:

1. Michel L Bushnell and Vishrani D Agrawal, "*Essentials of Electronic Testing for Digital, Memory and Mixed-signal VLSI Circuits*".
2. N. Jha& S.D. Gupta, "*Testing of Digital Systems*", Cambridge, 2003.
3. M. Abraham ovici etal, "*Digital System Testing and Testable Design*", Computer Science Press, 1990

MEC13V012 **ASIC DESIGN** **3 1 0 4**

OBJECTIVES

- To enable the students to understand and analyze the various types of ASICs and their design flow

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 12Hrs

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND I\O CELLS 12Hrs

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE ANDLOWLEVELDESIGNENTRY 12Hrs

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 12Hrs

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation, Introduction to JTAG.

UNIT-V ASIC CONSTRUCTION, FLOORPLANNING, PLACEMENT AND ROUTING 12Hrs

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow – global routing - detailed routing - special routing - circuit extraction - DRC.

Total No. of Hrs: 60

References:

1. M.J.S .Smith, "Application - *Specific Integrated Circuits* ", Addison -Wesley Longman Inc., 1997.
2. Andrew Brown, *" VLSI Circuits and Systems in Silicon*", McGraw Hill, 1991
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, "*Field Programmable Gate Arrays*" Kluwer Academic Publishers, 1992.

MEC13VE01 VLSI TECHNOLOGY 3 0 0 3

OBJECTIVES

- To enable the students to understand various design flow in VLSI and their applications in fuzzy systems

UNIT I VLSI DESIGN FLOW 9 Hrs

Design hierarchy concepts of regularity, modularity & locality VLSI Design styles - CMOS Fabrication Technology- Introduction, Fabrication Process flow- basic steps, CMOS n-well process, Advanced CMOS fabrication technologies, layout design rules-Introduction-Full – custom Mask Layout design –CMOS Layout design rules – CMOS inverter Layout design – Layout of CMOS NAND & NOR gates – Complex CMOS Logic gates

UNIT II PARASITIC EXTRACTION & PERFORMANCE ESTIMATION FROM PHYSICAL STRUCTURE 9 Hrs

Introduction – Reality with inter connection –MOSFET capacitances-interconnect capacitance estimation – interconnect resistance estimation

UNIT III CLOCK SIGNALS & SYSTEM TIMING 9 Hrs

On chip clock generation & distribution using ring & pierce crystal oscillator – non – overlapping clock signals and gate level implementation – H-tree clock distribution N/W – clock skew reduction – Zero – Skew clock routing N/W- Clock distribution N/W for DEC alpha µp chips

UNIT IV TESTABILITY OF INTEGRATED SYSTEMS-VLSI FOR FUZZY LOGIC SYSTEMS 9 Hrs

Design constraints – Testing – The rule of ten – terminology – Failures in CMOS – Combinational Logic Testing – Practical Ad-Hoc DFT guidelines – Scan design techniques- Integrated implementations of FLC, Digital implementation of FLC's, Analog implementation of FLC's, Mixed digital / analog implementations of Fuzzy systems, CAD automation for FLC DESIGN, NN implementing fuzzy systems.

UNIT V ARITHMETIC FOR DIGITAL SYSTEMS 9 Hrs

Introduction – notation systems – Principles of generation & propagation – 1 bit full adder – Enhancement Techniques for Adders – multi operand – Adders – Multiplication – Addition and Multiplication in Galois Fields GF(2n)

References: **Total No. of Hrs: 45**

1. Cheng., SZE., "*VLSI Technology*"., Prentice Hall of India,
2. Douglas A. Pucknell and Kamran Eshraghian, "*Basic VLSI Design Systems and Circuits*", Prentice Hall of India Pvt Ltd., 1993.
3. Horspool., Gorman., "*The ASIC Handbook*", Tata Mc Graw Hill Publications., 1999
4. Randall .L. Geiger and P.E. Allen, "*VLSI Design Techniques for Analog and Digital Circuits*", McGraw Hill International Company, 1990

MEC13VE02 OPTIMIZATION TECHNIQUES AND THEIR APPLICATIONS IN VLSI DESIGN

3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts of various optimization techniques and genetic algorithms to design VLSI systems

UNIT I STATISTICAL MODELING **9 Hrs**

Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom's model, Principal component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models

UNIT II STATISTICAL PERFORMANCE, POWER AND YIELD ANALYSIS **9 Hrs**

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT III CONVEX OPTIMIZATION **9 Hrs**

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Max- monomial fitting, Polynomial fitting.

UNIT IV GENETIC ALGORITHM **9 Hrs**

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi way Partitioning Hybrid genetic-encoding-local improvement-WDFR-Comparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.

UNIT V GA ROUTING PROCEDURES AND POWER ESTIMATION **9 Hrs**

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures. Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA Vs Conventional algorithm.

Total No of Hrs: 45

References:

1. Ashish Srivastava, Dennis Sylvester, David Blaauw "*Statistical Analysis and Optimization for VLSI: Timing and Power*", Springer, 2005.
2. Pinaki Mazumder, E., "Genetic Algorithm for VLSI Design, Layout and test Automation", Prentice Hall, 1998.
3. Stephen Boyd, Lieven Vanden berghe "Convex Optimization", Cambridge University Press, 2004.

MEC13VE03 EMBEDDED LINUX 3 0 0 3

OBJECTIVES

- To enable the students to understand the concepts of Embedded Linux basics and their applications

UNIT –I FUNDAMENTALS OF OPERATING SYSTEMS 8 Hrs

Overview of operating systems – Process and threads – Processes and Programs – Programmer view of processes – OS View of processes – Threads - Scheduling – Non preemptive and preemptive scheduling – Real Time Scheduling – Process Synchronization – Semaphores – Message Passing – Mailboxes – Deadlocks – Synchronization and scheduling in multiprocessor Operating Systems

UNIT – II LINUX FUNDAMENTALS 10 Hrs

Introduction to Linux – Basic Linux commands and concepts – Logging in - Shells - Basic text editing - Advanced shells and shell scripting – Linux File System –Linux programming - Processes and threads in Linux - Inter process communication – Devices – Linux System calls

UNIT –III INTRODUCTION TO EMBEDDED LINUX 8 Hrs

Embedded Linux – Introduction – Advantages- Embedded Linux Distributions - Architecture - Linux kernel architecture - User space – Linux startup sequence - GNU cross platform Tool chain

UNIT – IV BOARD SUPPORT PACKAGE AND EMBEDDED STORAGE 10 Hrs

Inclusion of BSP in kernel build procedure - The boot loader Interface – Memory Map – Interrupt Management – PCI Subsystem – Timers – UART – Power Management – Embedded Storage – Flash Map – Memory Technology Device (MTD) –MTD Architecture - MTD Driver for NOR Flash – The Flash Mapping drivers – MTD Block and character devices – mtdutils package – Embedded File Systems – Optimizing storage space – Turning kernel memory

UNIT – V EMBEDDED DRIVERS AND APPLICATION PORTING 9 Hrs

Linux serial driver – Ethernet driver – I2C subsystem – USB gadgets – Watchdog timer – Kernel Modules – Application porting roadmap - Programming with threads – Operating System Porting Layer – Kernel API Driver - Case studies - RT Linux – uCLinux

Total No. of Hrs: 45

References:

1. Dhananjay M. Dhamdhere, "*Operating Systems A concept based Approach*", Tata Mcgraw-Hill Publishing Company Ltd
2. Matthias Kalle Dalheimer, Matt Welsh, "*Running Linux*", O'Reilly Publications 2005
3. Mark Mitchell, Jeffrey Oldham and Alex Samuel "*Advanced Linux Programming*" New Riders Publications
4. P. Raghavan, Amol Lad , Sriram Neelakandan, "*Embedded Linux System Design and Development*", Auerbach Publications 2006
5. Karim Yaghmour, "*Building Embedded Linux Systems*", O'Reilly Publications 2003

MEC13VE04 INTRODUCTION TO MEMS SYSTEM DESIGN 3 0 0 3

OBJECTIVES

- To enable the students to learn the basic concepts of MEMS design and their applications

UNIT I INTRODUCTION TO MEMS 9 Hrs

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelerometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II MECHANICS FOR MEMS DESIGN 9 Hrs

Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III ELECTRO STATIC DESIGN 9 Hrs

Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. Bistable actuators.

UNIT IV CIRCUIT AND SYSTEM ISSUES 9 Hrs

Electronic Interfaces, Feedback systems, Noise, Circuit and system issues, Case studies – Capacitive accelerometer, Peizo electric pressure sensor, Modeling of MEMS systems, CAD for MEMS.

UNIT V INTRODUCTION TO OPTICAL AND RF MEMS 9 Hrs

Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues.

Total No. of Hrs: 45

References:

1. Stephen Santuria, "*Microsystems Design*", Kluwer publishers, 2000.
2. NadimMaluf,"*An Introduction to Micro Electro Mechanical System Design*", Artech House, 2000
3. Mohamed Gad-el-Hak, editor, "*The MEMS Handbook*", CRC press Baco Raton, 2000.
4. Tai Ran Hsu, "*MEMS & Micro Systems Design and Manufacture*" Tata McGraw Hill, New Delhi, 2002.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MEC13VE05 EMBEDDED NETWORKING 3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts of Embedded communication protocols in wireless communication

UNIT I EMBEDDED COMMUNICATION PROTOCOLS 8 Hrs

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming -ISA/PCI Bus protocols – Firmware

UNIT IIUSB AND CAN BUS 10 Hrs

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN

UNIT III ETHERNET BASICS 9 Hrs

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol

UNIT IVEMBEDDED ETHERNET 9 Hrs

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT V WIRELESS EMBEDDED NETWORKING 9 Hrs

Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing

Total No. of Hrs: 45

References:

1. Frank Wahid, Givargis "*Embedded Systems Design: A Unified Hardware/Software Introduction"*, Wiley Publications
2. Jan Axelson, "*Parallel Port Complete*", Penram publications.
3. Dogan Ibrahim, "*Advanced PIC Microcontroller Projects in C*", Elsevier 2008.
4. Jan Axelson "*Embedded Ethernet and Internet Complete*", Penram publications.
5. Bhaskar Krishnamachari, "*Networking wireless sensors*", Cambridge press 2005.

MEC13A006 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING 3 0 0 3

OBJECTIVES

- To enable the students to learn the concepts of parallel processing and their performances

UNIT – I THEORY OF PARALLELISM 9 Hrs

Parallel Computer models – the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks, Program and network properties – Conditions of parallelism.

UNIT – II PARTITIONING AND SCHEDULING 9 Hrs

Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures, Principles of scalable performance – performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

UNIT – III HARDWARE TECHNOLGIES 9 Hrs

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory – backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.

UNIT – IV PIPELINING AND SUPERSCALAR TECHNOLOGIES 9 Hrs

Parallel and scalable architectures, Multiprocessor and Multi computers, Multi vector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT – V SOFTWARE AND PARALLEL PROCESSING 9 Hrs

Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

Total No. of Hrs: 45

References:

1. Kai Hwang "*Advanced Computer Architecture*", McGraw Hill International 2001.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, "*Advanced Computer Architecture – A Design Space Approach*". Pearson Education, 2003.
3. Carl Homacher, ZvonkoVranesic, SefwatZaky, "*Computer Organisation*", 5th Edition, TMH, 2002.
4. David E. Culler, Jaswinder Pal Singh with Anoop Gupta "*Parallel Computer Architecture"* ,Elsevier, 2004.
5. John P. Shen. "*Modern Processor Design Fundamentals of Super Scalar Processors*", Tata McGraw Hill 2003.
6. Sajjan G. Shiva "*Advanced Computer Architecture*", Taylor& Francis, 2008.
7. V. Rajaraman, C. Siva Ram Murthy, "*Parallel Computers- Architecture and Programming*", Prentice Hall India, 2008.
8. John L. Hennessy, David A. Peterson, "*Computer Architecture: A Quantitative Approach*", 4th Edition, Elsevier, 2007.

MEC13VE06 DESIGN OF EMBEDDED CONTROL SYSTEM 3 0 0 3

OBJECTIVES

- To enable the students to design, develop and interface using real-time embedded technologies

UNIT – I EMBEDDED SYSTEM ORGANIZATION 9 Hrs

Embedded computing – characteristics of embedded computing applications – embedded system design challenges; Build process of Real time Embedded system – Selection of processor; Memory; I/O devices-Rs-485, MODEM, Bus Communication system using I2C, CAN, USB buses, 8 bit –ISA, EISA bus.

UNIT – II REAL-TIME OPERATING SYSTEM 9 Hrs

Introduction to RTOS; RTOS- Inter Process communication, Interrupt driven Input and Output –Non maskable interrupt, Software interrupt; Thread – Single, Multithread concept; Multitasking Semaphores.

UNIT – III INTERFACE WITH COMMUNICATION PROTOCOL 9 Hrs

Design methodologies and tools – design flows – designing hardware and software Interface. – System integration; SPI, High speed data acquisition and interface-SPI read/write protocol, RTC interfacing and programming;

UNIT – IV DESIGN OF SOFTWARE FOR EMBEDDED CONTROL 9 Hrs

Software abstraction using Mealy-Moore FSM controller, Layered software development, Basic concepts of developing device driver – SCI – Software - interfacing & porting using standard C & C++; Functional and performance debugging with benchmarking Real-time system software – Survey on basics of contemporary RTOS – VXWorks, UC/OS-II

UNIT –V CASE STUDIES WITH EMBEDDED CONTROLLER 9 Hrs

Programmable interface with A/D & D/A interface; Digital voltmeter, control- Robot system; - PWM motor speed controller, serial communication interface.

Total No. of Hrs: 45

References:

1. Steven F. Barrett, Daniel J. Pack, "*Embedded Systems – Design and Applications with the 68HC 12 and HCS12*", Pearson Education, 2008.
2. Raj Kamal, "*Embedded Systems- Architecture, Programming and Design*" Tata McGraw Hill, 2006.
3. Micheal Khevi, "*The M68HC11 Microcontroller Application in Control, Instrumentation& Communication*", PH New Jersey, 1997.
4. Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey, "*PIC Microcontroller and Embedded Systems-Using Assembly and C for PIC18*", Pearson Education, 2008.
5. Steven F. Barrett, Daniel J. Pack, "*Embedded Systems-Design & Application with the 68HC12 & HCS12*", Pearson Education, 2008.
6. Daniel W. Lewis, "*Fundamentals of Embedded Software*", Prentice Hall India, 2004.
7. Jack R Smith "*Programming the PIC microcontroller with MBasic*" Elsevier, 2007.

MEC13VE07 ADVANCED EMBEDDED SYSTEMS 3 0 0 3

OBJECTIVES

- To emphasize on hardware-software co design in embedded systems

UNIT I INTRODUCTION TO EMBEDDED HARDWARE AND SOFTWARE 9 Hrs

Terminology – Gates – Timing diagram – Memory – Microprocessor buses – Direct memory access – Interrupts – Built interrupts – Interrupts basis – Shared data problems – Interrupt latency - Embedded system evolution trends – Interrupt routines in an RTOS environment.

UNIT II SYSTEM MODELLING WITH HARDWARE/SOFTWARE PARTITIONING 9 Hrs

Embedded systems, Hardware/Software Co-Design, Co-Design for System Specification and modeling- Single-processor Architectures &,Multi-Processor Architectures, comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification, Hardware/Software Partitioning Problem, Hardware/Software Cost Estimation, Generation of Partitioning by Graphical modeling, Formulation of the HW/SW scheduling, Optimization.

UNIT – III HARDWARE/SOFTWARE CO-SYNTHESIS 9 Hrs

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

UNIT - IV MEMORY AND INTERFACING 9 Hrs

Memory: Memory write ability and storage performance – Memory types – composing memory – Advance RAM interfacing communication basic – Microprocessor interfacing I/O addressing – Interrupts – Direct memory access – Arbitration multilevel bus architecture – Serial protocol – Parallel protocols – Wireless protocols – Digital camera example.

UNIT V CONCURRENT PROCESS MODELS AND HARDWARE SOFTWARE CO-DESIGN 9 Hrs

Modes of operation – Finite state machines – Models – HCFSL and state charts language – state machine models – Concurrent process model – Concurrent process – Communication among process –Synchronization among process – Implementation – Data Flow model. Design technology – Automation synthesis – Hardware software co-simulation – IP cores – Design Process Model.

References: Total Hrs: 45

1. David. E. Simon, "*An Embedded Software Primer",* Pearson Education, 2001.
2. Tammy Noergaard, "*Embedded System Architecture, A comprehensive Guide for Engineers and Programmers"*, Elsevier, 2006
3. Raj Kamal, "*Embedded Systems- Architecture, Programming and Des*ign", TMH, 2006.
4. Frank Vahid and Tony Gwargie, "*Embedded System Design*", John Wiley & sons, 2002.
5. Steve Heath, "*Embedded System Design*", Elsevier, Second Edition, 2004.
6. Ralf Niemann, "*Hardware/Software Co-Design for Data Flow Dominated Embedded Systems*", Kluwer Academic Pub, 1998.
7. Jorgen Staunstrup, Wayne Wolf, "*Hardware/Software Co-Design: Principles and Practice*", Kluwer Academic Pub, 1997.

MEC13VE08 DISTRIBUTED EMBEDDED COMPUTING 3 0 0 3

OBJECTIVES

- To study and analyse embedded systems in JAVA based distributed environment

UNIT –I THE HARDWARE INFRASTRUCTURE 9 Hrs

Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.

UNIT –II INTERNET CONCEPTS 9 Hrs

Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

UNIT –III DISTRIBUTED COMPUTING USING JAVA 9 Hrs

IO streaming – Object serialization – Networking – Threading – RMI – multicasting – distributed databases – embedded java concepts – case studies.

UNIT – IV EMBEDDED AGENT 9 Hrs

Introduction to the embedded agents – Embedded agent design criteria – Behavior based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.

UNIT –V EMBEDDED COMPUTING ARCHITECTURE 9 Hrs

Synthesis of the information technologies of distributed embedded systems – analog/digital co-design – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system-on-chip – a new dynamic scheduling algorithm for real-time multiprocessor systems.

References: Total No. of Hrs: 45

1. Dietel & Dietel, "*JAVA How to Program*", Prentice Hall 1999.
2. Sape Mullender, "*Distributed Systems*", Addison-Wesley, 1993.
3. George Coulouris and Jean Dollimore, "*Distributed Systems – Concepts and Design*", Addison –Wesley 1988.
4. "*Architecture and Design of Distributed Embedded Systems*", Edited by Bernd Kleinjohann C-lab, University at Paderborn, Germany, Kluwer Academic Publishers, Boston, April 2001.