M. Tech. - VLSI Design & Embedded System Engineering – Part Time - 2007

Semester – I

Subject code	Subject	L	T	P	C
MMA101	*Applied Engineering Mathematics	3	1	---	4
MEC131	*Advanced Digital System Design	3	0	---	3
MEC133	*VLSI Design	3	0	---	3
				Total	**10**

Code	Equivalent of the previous years / Full-Time / Other departments
MMA101	MMA101
MEC105	MEC131
MEC106	MEC133

Semester – II

Subject code	Subject	L	T	P	C
MEC132	*Device Modeling	3	0	--	3
MEC134	*System modeling using Hardware Description Language (VHDL & Verilog)	3	1	--	4
MEC136	*Real-time Operating systems and System design using C/C++	3	0	--	3
MEC138	Circuit Design Lab - I		-	3	2
				Total	**12**

Code	Equivalent of the previous years / Full-Time / Other departments
MEC132	MEC122
MEC134	MEC123
MEC136	----------
MEC138	MEC124

Semester – III

Subject code	Subject	L	T	P	C
MEC231	*VLSI Technology	3	0	---	3
MEC202	*Advanced Digital signal processing	3	0	---	3
MEC235	DSP Architecture	3	0	---	3
MEC237	Circuit Design Lab – II	0	0	3	2
				Total	**11**

Code	Equivalent of the previous years / Full-Time / Other departments
MEC231	MEC121/MEC109
MEC202	MEC 233, MEC112, MEC 212
MEC235	----------
MEC237	----------

Semester – IV

Subject code	Subject	L	T	P	C
MEC232	*Computer Aided Design of VLSI Circuits	3	1	--	4
MEC234	*Microcontroller Architecture and Programming	3	1	---	4
MEC236	*Embedded System Design	3	1	---	4
MEC238	*Embedded System Design Lab	-	-	3	2
				Total	**14**

Code	Equivalent of the previous years / Full-Time / Other departments
MEC232	MEC125
MEC234	--------
MEC236	--------
MEC238	--------

Semester – V

Subject code	Subject	L	T	P	C
MEC331	*VLSI Testing and Verification	3	1	---	4
MEC333	*ASIC Design, SOC & FPGA Customization	3	1	---	4
MEC335	*Mixed Signal Processing	3	1	---	4
MEC337	*Mini – Project on Embedded System Design	-	-	4	4
				Total	**16**

Code	Equivalent of the previous years / Full-Time / Other departments
MEC331	----------
MEC333	----------
MEC335	--------
MEC337	---------

Semester – VI

Subject code	Subject	L	T	P	C

MEC332	*VLSI Design Lab	-	-- 3	2	
MEC334	*Project Work & Viva Voce	---	---	---	12

				Total	**14**

Code	Equivalent of the previous years / Full-Time / Other departments
MEC332	-------
MEC334	------

Note: * Core Subjects

Total Credits: 77

L: Lecture **T: Tutorial** **P: Practical** **C: Credit**

MMA101 APPLIED ENGINEERING MATHEMATICS 3 1 0 4

RANDOM PROCESS **12**

Random Variables – Density & Distribution Functions, Moments, Moment Generating Functions – Two – Dimensional Random Variables – Marginal & Conditional Distribution – Random Process – Stationary & Ergodic Process – Auto Correlation Cross Correlation – Properties – Power Spectral Density.

SPECIAL FUNCTIONS **12**

Series Solutions – Bessel's Equation – Bessal's Functions – Legendre's Equation – Legendre's Polynomial – Rodrigue's Formula – recurrence Relations – Generating functions & Orthogonal Property for Bessel's Function of the First Kind.

CALCULUS OF VARIATIONS **12**

Introduction – Euler's Equations – Functional Dependent on First and Second Derivatives – Brachistochrone Problem- Functional involving two or more Independent Variables – Isoperimetic Problem – variational Methods of Solving partial Differential Equations Rayleigh – Ritz Methods – Kantorovich Methods

LINEAR INTEGRAL EQUATIONS **12**

Different Types of Integral Equations – Fredholm & Volterra Integral Equations – Relation between Differential and Integral Equations – Green's Functions – Fredholm's Equations with Separable kernel – iterative Methods for Solving Equations of Second kind – properties of Symmetric Kernels.

INTRODUCTION TO FINITE ELEMENT METHOD **12**

Introduction – FEM – functions – Base Functions – Methods – of Approximation – Rayleigh – Ritz Method – Galerkin Method – Application to One – Dimensional & Two Dimensional Problem

Total No. of Hours : 60

Books for Study and Reference:

1. Hildebrand, F.B. "Methods of Applied Mathematics", PHI, New Delhi (1992)
2. Elsgolt.L., "Differential Equations & Calculus of Variations", Mir Pub Moscow, (1985).
3. Clarke.A.B., Disney, R.L, "Probability and Random Process", John Wiley, (1970).
4. Narayanan.S., et.al, "Advanced Mathematics for Engineering Students", Madras (1989).
5. Zienkienviez, O.C,. "Finite Element Methods in Engg. Sciences", McGraw Hill, London, (1989)
6. Papoulis, "Probability, Random Variables & Stochastic Process, McGraw Hill, New York (1991)
7. Petrovsky, L.G. "Lectures on Theory of Integral function", Mit Pub. Moscow (1971)
8. Andrews, L.A, "Special Functions for Scientists & Engineers", McGraw Hill, New York, (1992)

MEC105 ADVANCED DIGITAL SYSTEM DESIGN 3 0 0 3

ADVANCED TOPICS IN BOOLEAN ALGEBRA **9**

Shannon's expansion theorem, Conseusus theorem, Octal designation, Runmeasure, INHIBIT/INCLUSION / AOI / Driver / Buffer gates, Gate expander, Reed Muller expansion, synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.

THRESHOLD LOGIC **9**

Linear seperability, Unateness, Physical implementation, Dual comparability, Reduced functions, various theorems in threshold logic, Synthesis of single gate and multigate threshold Network.

SYMMETRIC FUNCTION **9**

Elementary symmetric functions, partially symmetric and totally symmetric function, Quin-Mc Cluskey decompositions method, Unity ratio symmetric ratio function, Synthesis of symmetric function by contact networks

SEQUENTIALLOGICCIRCUITS **9**

Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential Machines, State diagrams, State table minimization, incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards, Unger's theorem.

PROGRAMMABLE LOGIC DEVICES **9**

Basic concepts, Programming technologies, Programmable logic Element (PLE), Programmable Logic Array (PLA), Programmable Array Logic (PAL), Structure of Standard PLD's, Complex PLD's (CPLD). System Design Using PLD's – Design of combinational and sequentional circuits using PLD's, Programming PAL device using PALASM, Design of state machine using Algorithms State Machine (ASM) chart as a design tool.

Total No. of Periods:45

Reference Books:

1.William I. Fletcher, "AN Engineering Approach to Digital Design", Prentice Hall of India, 1996.
2.James E.Palmer, David E.Perlman, Introduction to Digital Systems", Tata McGraw Hill, 1996.
3.S.Devadas, A.Ghosh and K.Keutzer, "Logic Synthesis", McGraw Hill, 1994.
4.N.N.Biswas, "Logic Design Theory", Prentice Hall of India, 1993.

MEC106 VLSI DESIGN 3 0 0 3

MOS Technology and Circuits **9**

Mos Technology and VLSI, Process parameters and considerations for BJT, MOS and CMOS, Electrical properties of MOS circuits and Device modeling-MOS Circuit Design Process - MOS Layers, Stick diagram Layout diagram Propagation delays, Examples of combinational logic design, Sealing of MOS circuits, Capacitance Calculations

Digital Circuits and Systems **9**

Programmable Logic Array (PLA) and Finite State Machines, Design of ALUs, Memories and Registers.

Analog VLSI and High Speed VLSI **9**

Introduction to Analog VLSI, Realisation of Neural Networks and Switched capacitor filters, sub-micron technology and GaAs VLSI technology.

Hardware Description Languages **9**

VHDL background and basic concepts, Structural specifications of hardware design organisation and parameterisation.

VLSI Design **9**

VLSI applied to communication circuits, Filter design, VLSI for RF circuits, VLSI architectures for reduced critical path & low power design

Total No. of Periods = 45

References

1. Wayne Wolf, Modern VLSI Design, 2nd Edition, Prentice Hall, 1998.
2. Douglas A. Pucknell and Kamran Eshraghian, Basic VLSI Design Systems and circuits, Prentice Hall of India Pvt Ltd., 1993.
3. Randall .L.Geiger and P.E.Allen, VLSI Design Techniques for Analog and Digital Circuits, McGraw Hill International Company, 1990.
4. Amar Mukherjee, Introduction to NMOS and CMOS VLSI System Design, Prentice Hall, 1983.

MEC132 DEVICE MODELING 3 0 0 3

INTEGRATED PASSIVE DEVICES : 9
Types and structures of resistors and capacitors in monolithic technology – dependence of model parameters on structure.

INTEGRATED DIODES : 9
Junction and Schottky diodes in monolithic technologies – static and dynamic behavior – small and large signal models – SPICE models.

INTEGRATED BIPOLAR TRANSISTOR : 9
Types and structures in monolithic technologies – Basic model (EberMoll_-Cunmel – poon model – dynamic model, parasitic effects – SPICE model – parameter extraction.

INTEGRATED MOS TRANSISTOR : 9
MOS and PMOS Transistor – Threshold voltage -Threshold voltage equations – MOS device equations – basic DC equations Second order effects – MOS models Small signal AC Characteristics – MOSFET SPICE model level 1,2,3 and 4

SPICE MODELLING 9
Advanced Concepts large signal & low Signal modeling

Total no of hours : 45.

Reference
1. Daniel Foty, " MOSFET modeling with spice " prentice hall, 1997.
2. NeilWeste and Kamran Eshranghian " Principles of CMOS VLSI Design, A system Perspective", " Addition – Welslsy, 1993.
3. Jacob Millman & Arvin Millman, "Micro Electronics", McGraw Hill (Second Edi) 1987.
4. M.Styagi, John wiley " Introduction to Semi-conductor materials and devices ", New Edition

MEC134 System modeling using Hardware Description Languages 3 1 0 4

Unit I 12
VHDL & VERILOG Introduction and abridgment Date flow decryption – Structural-connected Blow

Unit II 12
Behaviour Description using Standard library – operators in VHDL Vector and scalar operations – Delay model – sequentional statement – signal and process

Unit – III 12
Implementation of combinational and sequential circuit using VHDL package

Unit – IV 12
Verilog and - Design function using Verilog –Levels of synthesizing Verilog Designing N/W using Verilog – Simple design – wires – wire assignments – Design

Unit – V 12
Test Benches –Response capture – RTL Verilog – If statement – Synthesis latches

Case Study
Design of universal asynchronous Receivers – Implementation of NAND – Latch. 16 bit counting, D type Edge triggered flip flop clock for counter – Fibonacci number generator- programmer using hand notation spice modeling of circuit

Total No. of hours : 60

Text Books
1. Mohammed Ismail., "Analog VLSI Integrated Circuits", Prentice Hall of India.,1998
2. Ashenden., "The Designers Guide to VHDL" Tata McGraw Hill Publications., 2nd Edition
3. Grey, Hurst Luwis, Mayer., "Analysis and Design of Analog Integrated Circuits" John Willey and Sons

MEC136 REAL-TIME OPERATING SYSTEMS &SYSTEM Programming using c/c++ 3 0 0 3

(a) Embedded system fundamentals 9
Why embedded systems are different? Characteristics of embedded systems and challenges in system design –design issues in embedded real-time systems, critical performance issues in embedded real-time systems. Software builds process- infinite loop process, compiling, linking & locating.
(b) Software porting issues on target hardware- Firmware/ device driver writing in c/c++/ assembly language, flashing the LED, program initialization, serial ports communication.
(c) Code optimization – increasing code efficiency, decreasing code size, reducing memory usage, limiting the usage of c++

Survey of software architectures 9
Round –robin, round-robin with interrupts, queues. Function- scheduling architecture, real time operating system architecture, scheduling architecture.

Elements of real time operating systems- tasks & task states, tasks & data, semaphores & shares data, message queues, mailboxes and pipes, timer functions, events, memory management and interrupt routines in an RTOS environment. **9**

Basic design using real-time operating systems principles, encapsulating semaphores & queues, hard real-time scheduling considerations, saving memory space, saving power. **9**

Embedded software development tools- host and target machines, linker/locators for embedded software, getting embedded software into the target system. Debugging techniques- testing on host system, instruction set simulators, the assert, macro using laboratory tools. **9**

Total Hrs: 45

References:

1. David e. Simon, "an embedded software primer", Pearson education, 1999.
2. Arnold s. Berger, "embedded systems design- an introduction to processes, tools & techniques ", CMP books, 2002.
3. Jean j. Labrosse, "embedded systems building blocks", CMP books, 2002.
4. Michael Barr, "programming embedded systems in c and c++", O'Reilly, 1999.
5. Wayne wolf, "computers as components- principles of embedded computing systems design", academic press, 2001.

MEC138 Circuit Design lab - I 0 0 3 2

1. Schematic Capture and PCB layout design using EDA tools.
2. System Design using Micro controllers.
3. Microcontroller based timers, Stepper motor controller, LCD & CRT Interfacing
4. System design using 16 bit Microprocessors.
5. SPICE simulation of electronic circuits.
6. Design of Power electronic circuits – SMPS, High Frequency DC/DC Converters using Power MOSFET

Total No. Of Periods: 45.

MEC231 VLSI TECHNOLOGY 3 0 0 3

VLSI Design flow **9**

Design hierarchy concepts of regularity, modularity & locality VLSI Design styles - CMOS Fabrication Technology- Introduction, Fabrication Process flow- basic steps, CMOS n-well process, Advanced CMOS fabrication technologies, layout design rules-Introduction-Full – custom Mask Layout design –CMOS Layout design rules – CMOS inverter Layout design – Layout of CMOS NAND & NOR gates – Complex CMOS Logic gates

Parasitic extraction & performance estimation from physical structure **9**

Introduction – Reality with inter connection –MOSFET capacitances-interconnect capacitance estimation – interconnect resistance estimation

Clock signals & system timing **9**

On chip clock generation & distribution using ring & pierce crystal oscillator – non – overlapping clock signals and gate level implementation – H-tree clock distribution N/W – clock skew reduction – Zero – Skew clock routing N/W- Clock distribution N/W for DEC alpha µp chips

Testability of Integrated systems-VLSI for Fuzzy logic systems **9**

Design constraints – Testing – The rule of ten – terminology – Failures in CMOS – Combinational Logic Testing – Practical Ad-Hoc DFT guidelines – Scan design techniques- Integrated implementations of FLC, Digital implementation of FLC's, Analog implementation of FLC's, Mixed digital / analog implementations of Fuzzy systems, CAD automation for FLC DESIGN, NN implementing fuzzy systems.

Arithmetic for Digital systems **9**

Introduction – notation systems – Priciples of generation & propagation – 1 bit full adder – Enhancement Techniques for Adders – multi operand – Adders – Multiplication – Addition and Multiplication in Galois Fields GF(2n)

Total number of hours: 45

Text Books:

1. Cheng., SZE., "VLSI Technology"., Prentice Hall of India,
2. Douglas A. Pucknell and Kamran Eshraghian, "Basic VLSI Design Systems and circuits", Prentice Hall of India Pvt Ltd., 1993.
3. Horspool., Gorman., "The Asic Handbook"Tata Mc Graw Hill Publications., 1999
4. Randall .L.Geiger and P.E.Allen, VLSI Design Techniques for Analog and Digital Circuits, McGraw Hill International Company, 1990

MEC202 ADVANCED DIGITAL SIGNAL PROCESSING 3 0 0 3

Discrete random signal processing **9**

Discrete Random Process, Expectation, Variance, Co-Variance, Scalar Product, Energy of Discrete Signal-Parseval's Theorem, Wiener Khintchine Relation-Power Spectral Density –Periodogram – Sample Autocorrelation-Sum Decomposition Theorem, Spectral Factorization Theorem – Discrete Random Signal Processing by Linear Systems-Simulation of White Noise – Low Pass Filtering of White Noise.

Spectrum Estimation **9**

Non-Parametric Methods-Correlation Method – Co-Variance Estimator – Performance Analysis of Estimators – Unbiased, Consistent Estimators – Periodogram Estimator – Barlett Spectrum Estimation – Welch Estimation – Model based Approach – AR, MA, ARMA Signal Modeling – Parameter Estimation using Yule-Walker Method.

Linear Estimation and Prediction **9**

Maximum likelihood criterion-efficiency f estimator – Least mean squared error criterion – Wiener filter – Discrete Wiener Hoff equations – Recursive estimators-Kalman filter – Linear prediction, prediction error-whitening filter, inverse filter – Levinson recursion, Lattice realization, and Levinson recursion algorithm for solving Teoplitz system of equations.

Adaptive Filters **9**

FIR adaptive filters – Newton's steepest descent method-adaptive filter based on steepest descent method – Widrow Hoff LMS adaptive algorithm – Adaptive channel equalizations – Adaptive echo chancellor – Adaptive noise cancellation – RLS adaptive filters –Exponentially weighted RLS – sliding window RLS – Simplified IIR LMs adaptive filter

Multirate Digital Signal Processing **9**

Mathematical description of change of sampling rate – Interpolation and Decimation –continuous time model – Direct digital domain approach - Decimation by an integer factor – Interpolation by an integer factor – single and multistage realization - Poly phase realization – Application to sub band coding – Wavelet transform and filter bank implementation of wavelet expansion of signals.

Total No. of Hours = 45

Textbooks:

1.Monson H.Hayes, Statistical Digital Signal Processing and Modelling, John Wiley and Sons, Inc., New York, 1996

Reference Books

1. Sopocles J.Orfanidis, Optimum Signal Processing, McGraw Hill, 1990.
2. John G.Proakis, Dimitris G.Manolais, Digital Signal Processing Prentice Hall of India, 1995.

MEC235 DSP ARCHITECTURE 3 0 0 3

Digital signal processing and DSP systems: **9**

Introduction- advantages of DSP, characteristics of DSP systems, classes of DSP applications, numeric representations and arithmetic, Fixed-point verses Floating point, Native data word Width, extended precision, Floating point emulation and block floating point, IEEE -754 Floating Point, relationship between

data word size and instruction word size. Data path and instruction set- fixed point data paths, floating point data paths, special function units, instruction types, registers, parallel move support.

Memory architecture & addressing **9**

Memory structures, features of reducing memory access requirements, addressing- implied addressing, immediate data memory direct addressing, register direct addressing, register indirect addressing, short addressing modes. Execution- Control hardware looping, interrupts, stacks, relative branch support. Pipelining and performance, pipelining depth, interlocking, branch effects, interrupt effects, pipeline programming models.

Architectures and features of simple, fixed and floating point processors **9**

TMS320 C1x, TMS320 C2x, TMS320 C4x, TMS320 C5x, TMS320 C54x. VLIW architecture, register file architecture, memory architecture, branch architecture in DSP processors.

DSP Development tools **9**

Assemblers, simulator cross compilers- their features

Designing DSP based systems with ADC, ADC memory and interfacing consideration & future trends. **9**

Total No. of Periods : 45

Reference books:

1. EC Jfeachor and B. W. Jervis, "A Practical Approach", Addison Wesley 1993
2. Phil lapsley, Jeff Bier, Amit shoham and Edward A. lec, " DSP processor Fundamentals, architectures and features"
3. Users manuals of various fixed and floating point DSP's, Application guides from DSP manufactures.
4. selected papers from IEEE Journals
5. TI Website [http://www.ti.com]

MEC 237 CIRCUITS DESIGN LABORATORY – II **0 0 3 2**

Design the following modules using verilog and VHDL.

1. Flip- flops - D Flipflop; T Flipflop; JK Flipflop; RS Flipflop
2. Adders - a. Half- adder; b. Full- adder; c. CLA
3. Multiplexer - ▪ 4:1 multiplexer; ▪ 8:1 multiplexer
4. decoder
5. encoder
6. ALU
7. counters - ▪ 4 bit binary up down counter; ▪ Mod- N counters; ▪ Counter with parallel load and clear facility
8. shifts registers - ▪ Serial in serial out; ▪ Serial in parallel out; ▪ Parallel in series out; ▪ Parallel in parallel out
9. Mealy & moore machines
10. RAM & ROM
11. Sequence detector - ▪ 1011; ▪ 10101

MEC232 COMPUTER AIDED DESIGN OF VLSI CIRCUITS **3 1 0 4**

UNIT – I **12**

VLSI Methodologies – VLSI Physical Design Automation – Design and Fabrication of VLSI Devices – Fabrication process and its impact on Physical Design.

UNIT – II **12**

VLSI Design Automation Tools - Data structures and Basic Algorithms – Algorithms Graph Theory and compuptional complexity – Tractable and Intractable problems

UNIT – III **12**

General purpose methods for combinational optimization – Partitioning – Floor planning and pin assignment – placement – Routing

UNIT – IV **12**

Simulation – Logic synthesis – Verification – High-level synthesis – compaction.

UNIT – V **12**

Physical Design Automation of FPGAs, MCMS – VHDL – Verilog - Implementation of simple circuits using VHDL and Verilog packaging

Case Study;

Floor planning billion-gate design. Test vector generation design for testing fan et coverage **12**

Total No. of Periods : 60

Text Books :

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation". 1999.
2. S.H.Gerez, "Algorithms for VLSI Design Automation",1998.

MEC234 Microcontroller Architecture & Programming 3 1 0 4

Unit I **12**

(a) basic concepts- a black box introduction to microprocessors, block diagrams and system organization of typical microcomputers and embedded systems. Computer programs at the machine language level, RISC vs. CISC microprocessor architectures, Harvard and von Neumann architectures, varieties of memory-ROM, RAM, EPROM, EEPROM, FLASH, NVRAM, clocks and timers, system bus concepts(address bus, data bus, control bus)

(b) an overview of the architecture of 8051 of microcontrollers

(c) Basics of assembly language programming- bits, bytes and machine codes, manipulating registers (loading, incrementing contents, storing contents of some register in memory), jumping to and continuing execution at some specific address, writing assembling and debugging simple assembly language programs, driving a simple LED display.

Unit II **12**

Structured programming in assembler- Loops and counters, delay loops, structured code- modules, subroutines and stack operations, logical instructions (AND, OR, XOR, bit shifting). Doing arithmetic in assemble – arithmetic instructions and the ALU, simple integer arithmetic, higher precision integer arithmetic, an overview of floating point arithmetic techniques, an overview of techniques for calculating trigonometric and logarithmic functions.

Unit III **12**

Fundamentals of interfacing- Input/output ports (i/o) ports **(**serial i/o ports, parallel i/o ports), analog to digital (a/d) and digital to analog (D/A) conversion, programmable timers, interrupt handling, serial I/O, synchronous vs. asynchronous serial I/O, asynchronous transmission format, synchronous transmission format (SDLC), RS-232, terminal interfacing, modem interfacing, bit banging.

Unit IV **12**

Working with an embedded stack**:** Porting issues, systems requirements, integrating with other tools. Working with an operating system, memory management, testing

Unit V **12**

Further practical interfacing skills & software development tools**-** driving high current and high voltage devices, " pin expansion" techniques for data acquisition and control, working with the 12C bus, working with the SPI bus, working with the CAN bus. Assemblers, compilers, interpreters, C as a programming language for microcomputer systems.

Total No. of Periods : 60

Text book:

1. Steve heath *embedded System Design*, Newnes, ISSBN 0-7506-3237-2, 1997.

References:

1. David E. Simon, *An embedded software primer*, Addison Wesley, ISBN 0- 201-61569-X, 1999.
2. Michabel barr, *Programming Embedded Systems in C and C++*, O'Reilly, ISSBN 1-56592-354-5, 1999.
3. Stuart, R. Ball, *Debugging embedded microprocessor systems*, Newnes, ISSBN 0-7506-9990-6, 1998.
4. Nikitas Alexandridis, *design of microprocessor- based systems*, prentice hall, ISSBN 981-4009-48-2, 1997.

MEC 236 Embedded system design 3 1 0 4

Unit I **12**

(a) introduction, motivation. Soc development, etc. design methodologies (hw/sw co-design…)

(b) Specification: - imperative languages- programming lang. (c, c++), hardware description (VHDL, system c), - synchronous languages – esterel, signal, LUSTRE,…

Unit II **12**

Computational models (design representations)- data-flow based- data flow process networks, khan process networks, etc.)- control flow based-FSM, Petri nets, state charts, etc.- control/data-flow design representations.

Unit III **12**

(a) System partitioning (estimation, partitioning methods, etc.); (b) Allocation, assignment and scheduling- static scheduling,- dynamic scheduling.

Unit IV **12**

(a) Interface synthesis. (b) Testability.

Unit V **12**

Low-power design.

Total No. of Periods : 60

Text book:

W.wolf,"computers as components: principles of embedded computing systems design", Morgan Kaufman publisher, 2001, ISBN 1-55860-541-x (case), ISBN 1-55860-693-9 (paper)

MEC 238 Embedded system design lab 0 0 3 2

Major topics include the following:

(1) 8- bit microcontrollers
(2) Digital signal processors (DSPs)
(3) Programmable logic devices/FPGA.

MEC331 VLSI Testing & Verification 3 1 0 4

Introduction to Testing **12**

Introduction- Digital and Analog Testing, Types of Testing, Testing Equipments, test Economics.

Fault Modeling and Simulation **12**

Introduction, Levels of Fault Models, Simulation for Design Verification and test Evaluation, Modeling Circuits for Simulation, algorithms for fault simulation.

Test Generation **12**

Combinatorial Circuit Test Generation, Sequential Circuits test generation**.**

Analog & Mixed Signal Testing **12**
Memory Test - Memory Test Levels, Memory Testing, Definitions, Static ADC and DAC Testing Methods.

Design for Testability **12**
DFT Fundamentals, BIST Fundamentals, System Test and architecture, Future of Testing.

Total No. of Periods: 60

Reference :
Michel L Bushnell and Vishwani D Agrawal, "Essentials of electronic testing for Digital, memory and Mixed-signal VLSI circuits.

MEC 333	**ASIC Design, SOC & FPGA Customization**	**3**	**1**	**0**	**4**

INTRODUCTION TO ASICS AND ASIC LIBRARY DESIGN **12**
Types of ASICs- design flow, logical effort- library cell design- library architecture, gate array design, standard cell design, data-path cell design.

PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABL ASIC I/O CELLS **12**
anti fuse- static RAM- EPROM and EEPROM technology- PREP benchmarks- actel ACT-Xilinx LCA- altera FLEX- altera MAX, DC & AC inputs and outputs- clock and power inputs- Xilinx i/o blocks.

PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY **12**
Actel ACT- Xilinx LCA – Xilinx EPLD- Altera MAX 5000 and 7000 – Altera MAX 9000 – Altera FLEX – Design systems – logic synthesis – Half gate ASIC – Schematic entry – Low level design language – PLA tools – EDIF – CFI design representation.

SOC **12**

Case study: **12**
FPGA implementation of RS232C, RISC Processor.

Total No. of Periods : 60

Text books:
1. M. J. S. Smith, - "application – specific integrated circuits"- Addison- Wesley Longman inc., 1997.

References:

1. Andrew brown.- "VLSI circuits and systems in silicon", McGraw hill, 1991.
2. S. D. Brown, R. J. Rox, Z. G. Uranesic, "Field programmable gate arrays"- Kluever academic publishers, 1992.
3. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and information processing" , Mc Graw hill, 1994.
4. S. Y. Kung, H. J. Whilo house, T. Kailash, "VLSI and modern signal processing", prentice hall, 1985.
5. Jose E. France, Yannis Tsividis, " Design of analog – Digital VLSI Circuits for Telecommunication and signal processing", Prentice Hall, 1994

MEC 335	**Mixed-Signal Processing Systems**	**3**	**1**	**0**	**4**

Major topics include the following:

CONTENTS

System level design - Interpolation, decimation, and multirate systems - Synthesis of FIR filters - Synthesis of IIR filters - Finite wordlength effects - Single-amplifier active RC filters - Amplifiers and comparators - Tuning of Continuous-time integrated active filters - Sample-and-hold operation and circuits - Analog-to-digital converters-Digital-to-Analog conversion techniques

MEC 337	**Mini-project on VLSI design** Design of ASIC using cadence	**-**	**-**	**4**	**4**

MEC332	**VLSI DESIGN LAORATORY**	**0**	**0**	**3**	**2**

1. Design and testing of Flip flops
2. Design and testing of registers, counters
3. Design and testing of RAM, ROM Single Cells
4. Design and testing of memory units
5. Design and testing of circuits for combinational logic circuits
6. Design and testing of programming logic arrays
7. Design and testing of adders, multipliers
8. Design and testing of synchronous counters
9. Design and testing of A/D, D/A counters
10. Design and testing of applications based on synchronous logic.